

B550 AORUS ELITE AX V2

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2015.12.30--B.L

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TitleCOVER SHEET

SizeCustom

Document NumberB550 AORUS ELITE AX V2

Rev1.0

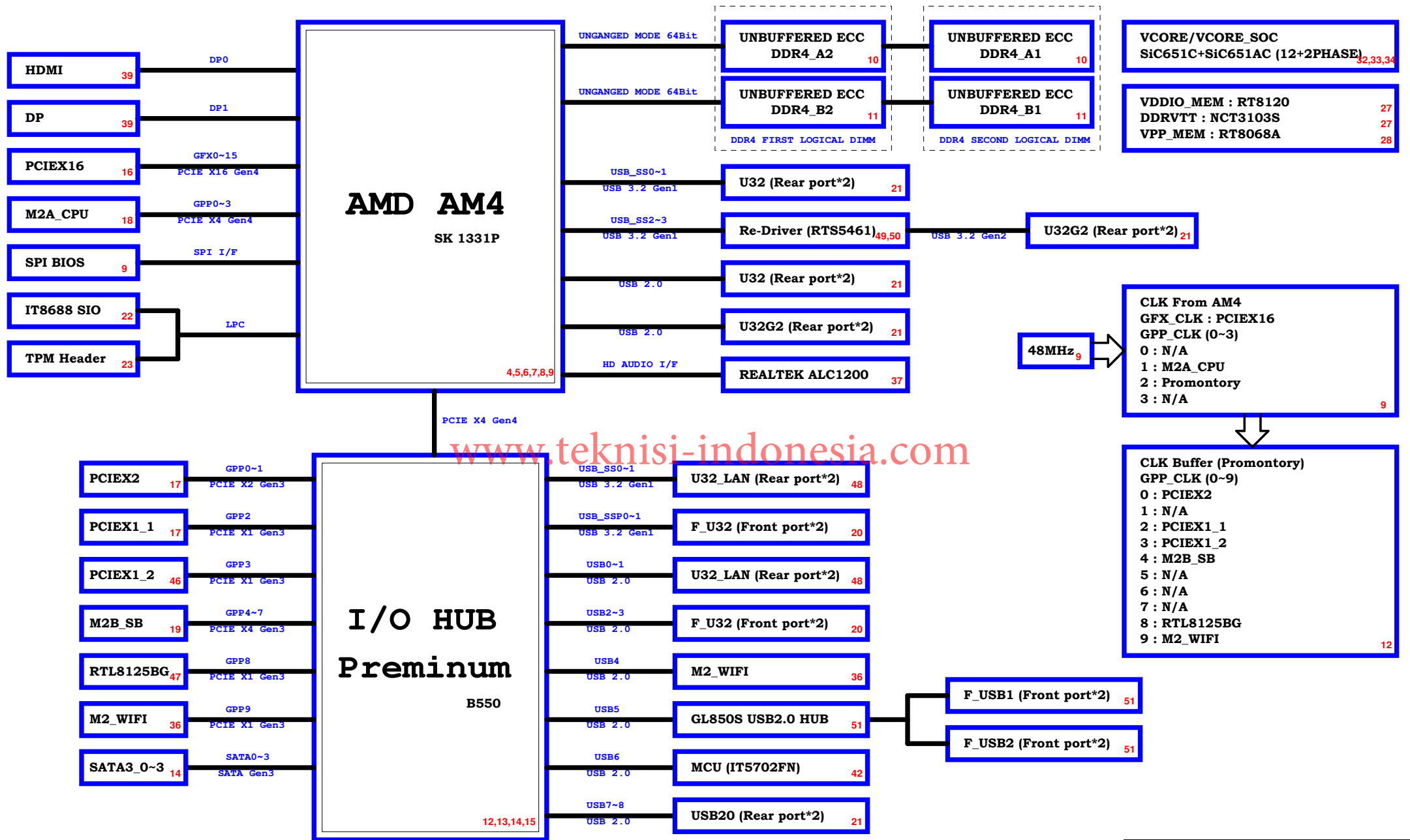
DateMonday, July 27, 2020

Sheet1

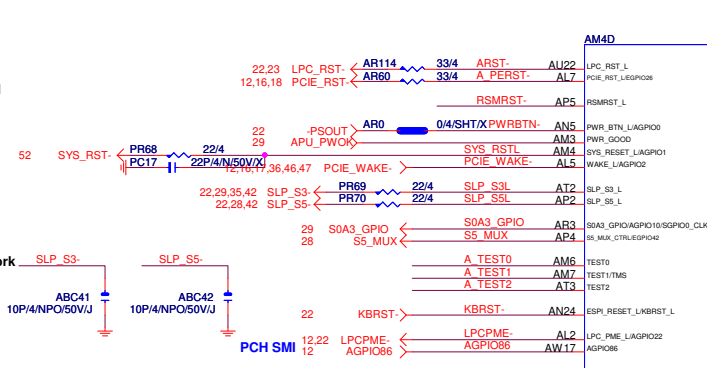
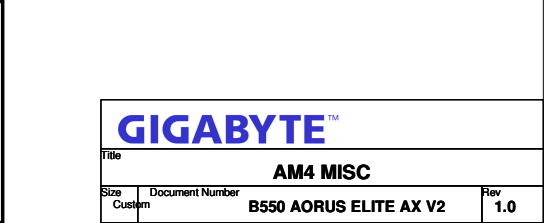
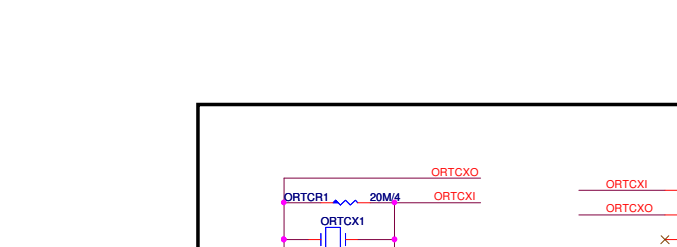
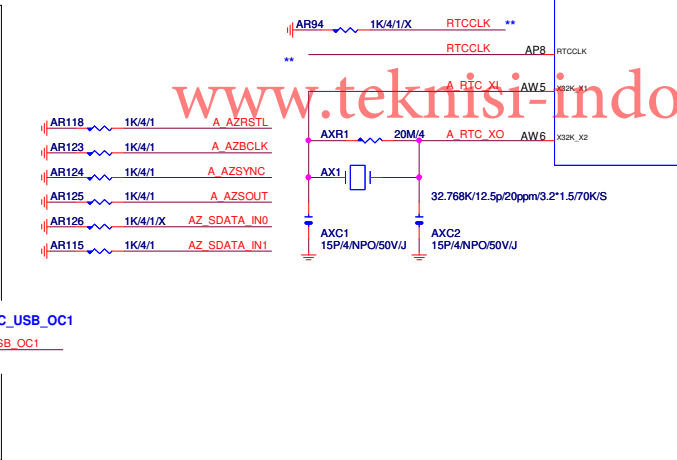
of52

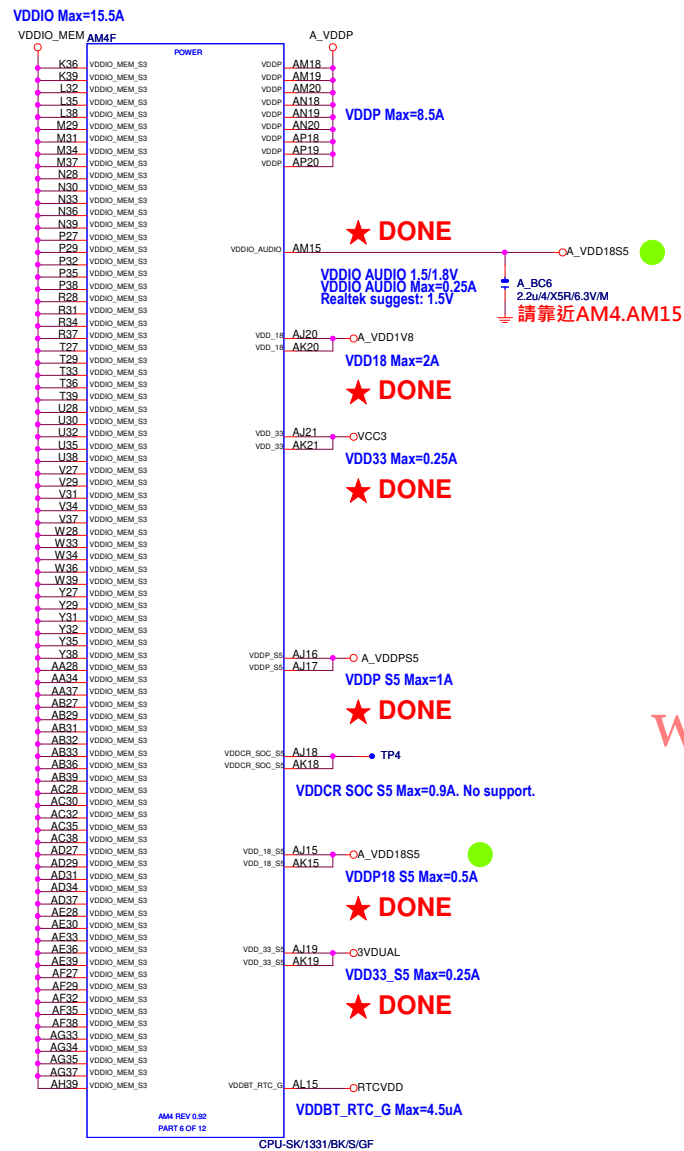
A vertical line with points A, B, C, and D marked from bottom to top. A horizontal arrow points from point B to the right.

BLOCK DIAGRAM



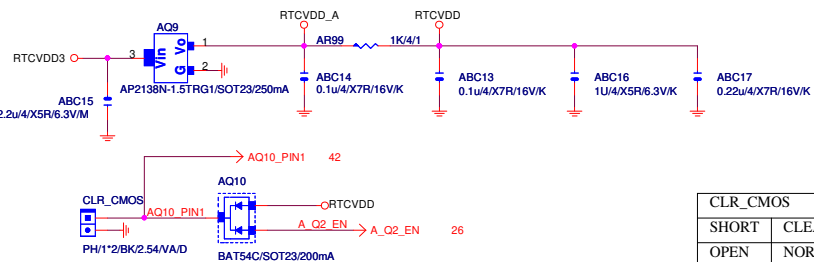
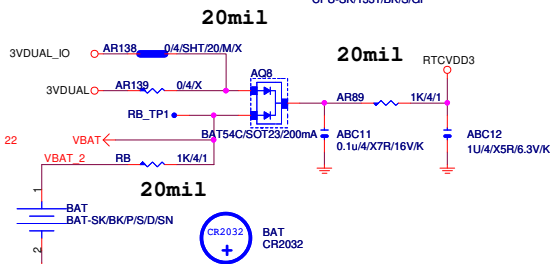
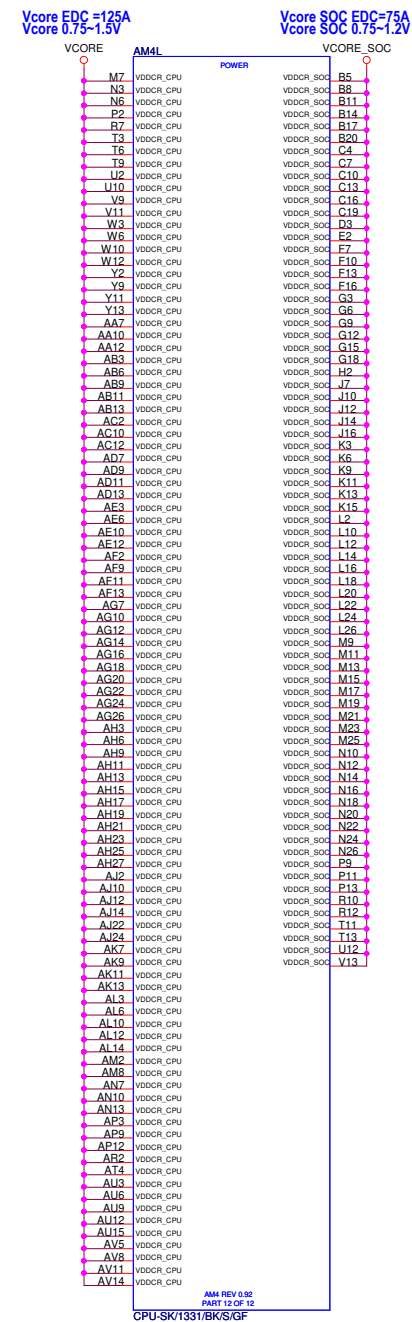


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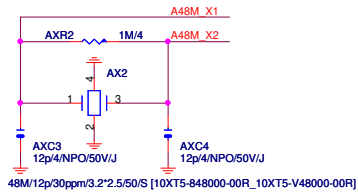
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CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL
NOT ADD ICT FOR RTCVDD PIN	

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Title CPU POWER & GND			
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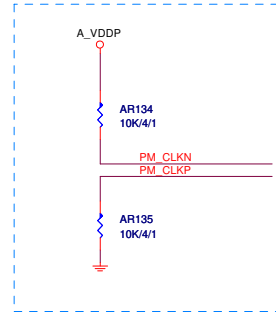


AM4 STRAP

	SPI_CLK	LFRAME	SYS_RST	LPC_CLK0	LPC_CLK1
PULL HIGH	Internal clock mode	SPI ROM	Normal reset mode	PSP modify SPI page reg bits[24:24]	Use 48MHz crystal clock
PULL LOW	Extal clock mode	LPC ROM	Short reset mode	PSP not modify SPI page reg bits[24:24]	Use 100MHz extl clock input.

Bule: default

pull up and pull down to the clock from CPU to X570 clock FOR INTERNAL CLOCK GEN project.



X16 Slot

16 A_GFX_CLKP < AF6 GFX_CLKP
16 A_GFX_CLKN < AE7 GFX_CLKN

M.2 Socket

18 M2A_CLKP < AH4 GPP_CLK1P
18 M2A_CLKN < AH5 GPP_CLK1N

Promontory

12 PM_CLKP < AH7 GPP_CLK2P
12 PM_CLKN < AH8 GPP_CLK2N

GPP0 input provides a clock input that replaces the internally generated 100Mhz based clock used as the reference for the CCLK PLL and divisor logic. GPP1 input should include spread spectrum modulation.

Del LPC_CLK0

23 DB_CLK < AR91 104 LPC_CLK0 AU20 LPCLK0/EGPIO74
22 LPC_CLK1 < AR69 224 LPC_CLK1 AU19 LPCLK1/EGPIO75

22,23 LAD0 < LAD0 AW20 LAD0/EGPIO104
22,23 LAD1 < LAD1 AV21 LAD1/EGPIO105
22,23 LAD2 < LAD2 AT21 LAD2/EGPIO106
22,23 LAD3 < LAD3 AT20 LAD3/EGPIO107
22,23 LFRAME < LFRAME AW18 LFRAME/EGPIO109
22,23 LDRO0 < LDRO0 AT15 ESPI_ALERT_LLDRQ0_LEGPIO108
22,23 SERIRQ0 < SERIRQ0 AW21 SERIRQ0/EGPIO87
22,23 ASPIC021 < ASPIC021 AV18 LAD0/EGPIO108
24 ASPIC021 < ASPIC021 AT18 EGPIO75

AGPIO21 FOR EXTREME USE

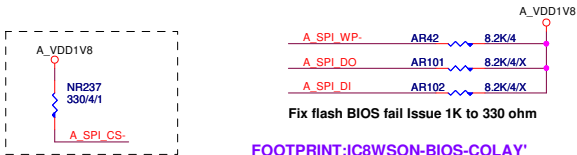
A SPI_CLK < AR56 224 SPI_CLK AW14 SPI_CLK/ESPI_CLK/EGPIO117
* A SPI_CS < AR57 224 SPI_CS AT17 SPI_CS1/EGPIO118

A SPI_DI < AR58 224 SPI_DI AW15 SPI_CS2/ESPI_CS/EGPIO119
A SPI_DO < AR59 224 SPI_DO AU14 SPI_DIESPI_DAT1/EGPIO120
A SPI_WP < AR128 224 SPI_WP AU16 SPI_DOESPI_DAT0/EGPIO121
A SPI_HD < AR129 224 SPI_HD AV15 SPI_WP_L/ESPI_DAT0/EGPIO122
18 M2_DEVSLP < M2_DEVSLP AU17 SPI_HOLD_L/ESPI_DAT0/EGPIO123

AM REV 6.12
PART 5 OF 12

CPU-SK/1331/BK/S/GF

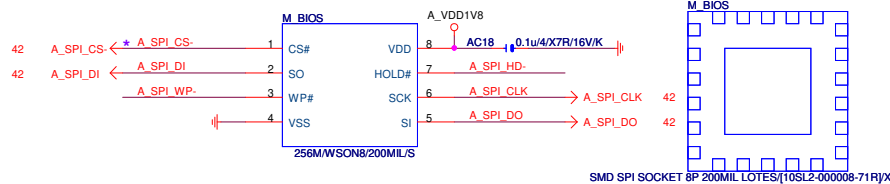
★1.8V SPI ROM USE



FOOTPRINT:IC8WS0N-BIOS-COLAY'

FOOTPRINT:IC8WS0N-BIOS-COLAY'

Single (128Mx1)
Layout colay 256Mx1



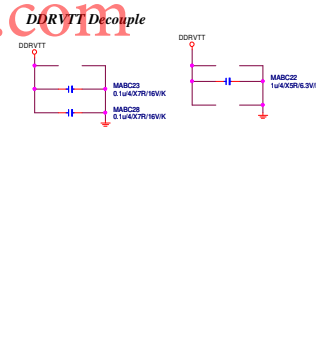
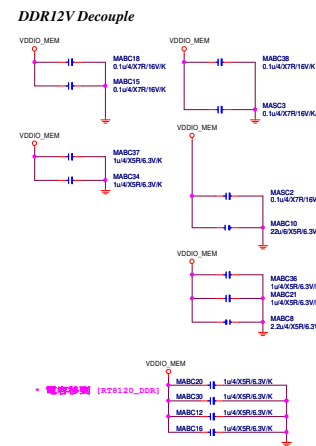


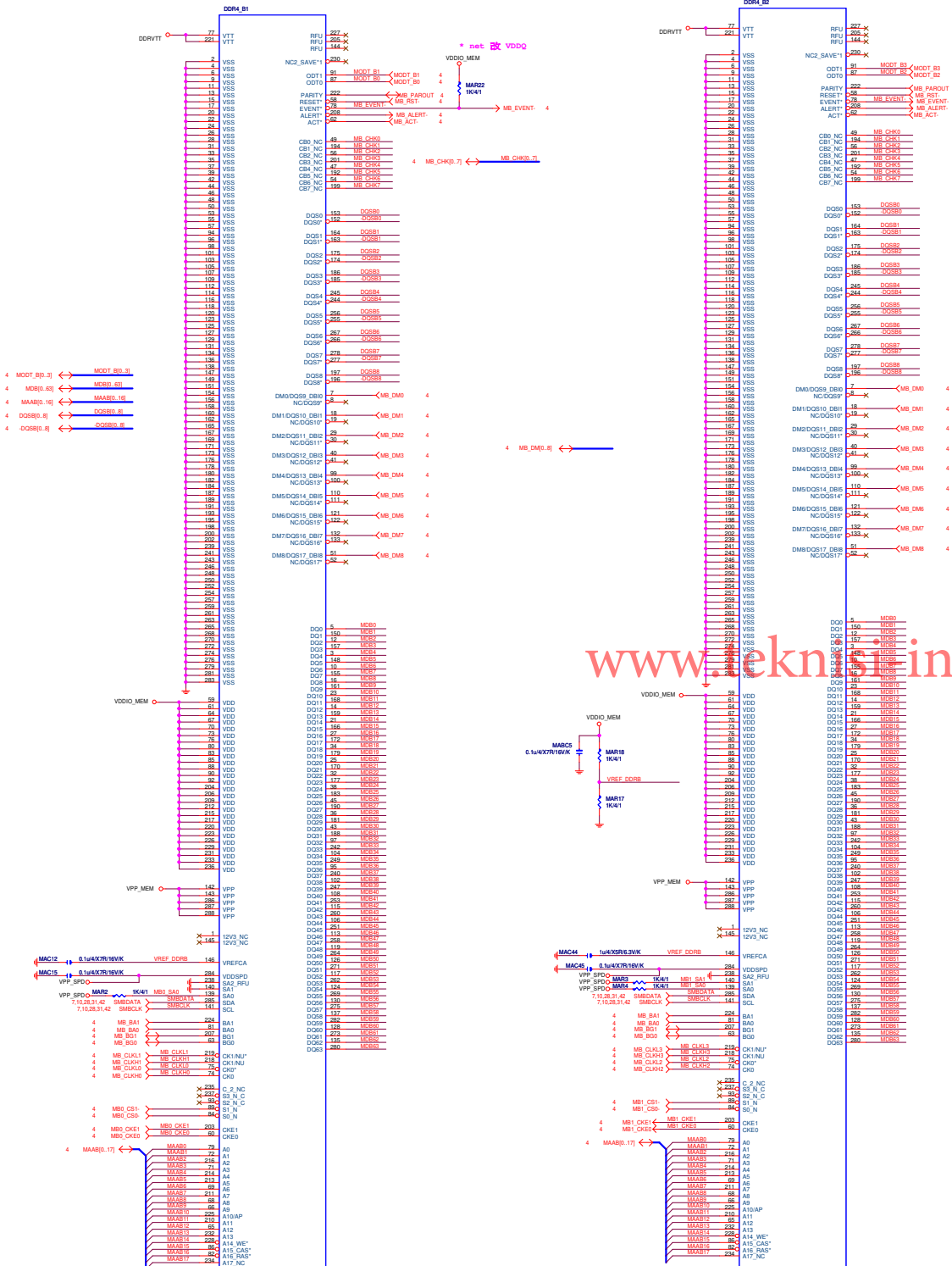
雙耳扣DDR4

DDR4-288P-STH-36C24P
DDR4-288P-34C22P-3

CHANNEL A0
SA2:0=000

CHANNEL A1
SA2:2=010





CHANNEL B0
SA2:1=001



CHANNEL B1
SA2:3=011

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DDR4 CHANNEL B			
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USB port power control 9:0
(VCC3). Output.

U1B
AB7 PPON_0
AE8 PPON_1
AD9 PPON_2
AC8 PPON_3
AB8 PPON_4
AF9 PPON_5
AE9 PPON_6
AC9 PPON_7
AE7 PPON_8
AD7 PPON_9

20,35 -USBOC_F1> -USBOC_F1< Y5 USB_OC1N
-USBOC_R1 AE6 USB_OC2N
-USBOC_F1 AD6 USB_OC3N
-USBOC_R1 AB6 USB_OC4N
-USBOC_F1 AA6 USB_OC5N
48 -USBOC_R1> -USBOC_R1< AE7 USB_OC7N

PR62 12.1K/4/1 P_UREXT AB11 UREXT

48 P_SSP_RX2P> P_SSP_RX2P AC16 USB_SS_RXP0
48 P_SSP_RX2N> P_SSP_RX2N AD16 USB_SS_RXN0
35 P_SSP_RX3P> P_SSP_RX3P AC17 USB_SS_RXP1
35 P_SSP_RX3N> P_SSP_RX3N AB17 USB_SS_RXN1

20 P_SSP_RX0P> P_SSP_RX0P AD12 USB_SS_RXP0
20 P_SSP_RX0N> P_SSP_RX0N AC12 USB_SS_RXN0
20 P_SSP_RX1P> P_SSP_RX1P AD14 USB_SS_RXP1
20 P_SSP_RX1N> P_SSP_RX1N AC14 USB_SS_RXN1

B550

218-0891014-00/S

X57

USB32G2	USB20	USB_OC
0	0	0
1	1	1
USB32G1		
0	2	2
1	3	3
	4	4
	5	5
	6	6
	7	7
	8	7
	9	7

USB Controller 0: USB20 [0:5], USB30 [0:3]

USB Controller 1: USB20 [6:11], USB30 [4:7]

USB30G2	USB20
0	4
1	4
2	5
3	5
4	9
5	8
6	7
7	6

USB30_I211 Lan

F_USB 30_2

F_USB 30_1

FRONT TYPE C

USB_HSDP0 AF1 P_HSDP0 P_HSDP0 20
USB_HSDN0 AF2 P_HSDN0 P_HSDN0 20
USB_HSDP1 AE1 P_HSDP1 P_HSDP1 20
USB_HSDN1 AE2 P_HSDN1 P_HSDN1 20
USB_HSDP2 AB1 P_HSDP2 P_HSDP2 48
USB_HSDN2 AB2 P_HSDN2 P_HSDN2 48
USB_HSDP3 Y1 P_HSDP3 P_HSDP3 35
USB_HSDN3 Y2 P_HSDN3 P_HSDN3 35
USB_HSDP4 AF3 P_HSDP4 P_HSDP4 36
USB_HSDN4 AF4 P_HSDN4 P_HSDN4 36
USB_HSDP5 AD3 P_HSDP5 P_HSDP5 51
USB_HSDN5 AD4 P_HSDN5 P_HSDN5 51
USB_HSDP6 AC1 P_HSDP6 P_HSDP6 42
USB_HSDN6 AC2 P_HSDN6 P_HSDN6 42
USB_HSDP7 AB3 P_HSDP7 P_HSDP7 21
USB_HSDN7 AB4 P_HSDN7 P_HSDN7 21
USB_HSDP8 AA3 P_HSDP8 P_HSDP8 21
USB_HSDN8 AA4 P_HSDN8 P_HSDN8 21
USB_HSDP9 AF5
USB_HSDN9 AE5

F_USB30

U32_LAN

F_TYPEC

M.2 WIFI

USB2.0 HUB (Front USB 2.0)

MCU

USB20

USB 3.2 Gen 1

USB_SS_TXP0 AF17 P_SSP_TX2P P_SSP_TX2P 48
USB_SS_TXN0 AE17 P_SSP_TX2N P_SSP_TX2N 48
USB_SS_TXP1 AE18 P_SSP_TX3P P_SSP_TX3P 35
USB_SS_TXN1 AE18 P_SSP_TX3N P_SSP_TX3N 35

F_USB30_1

USB 3.2 Gen 2

USB_SS_TXP0 AE13 P_SSP_TX0P P_SSP_TX0P 20
USB_SS_TXN0 AF13 P_SSP_TX0N P_SSP_TX0N 20
USB_SS_TXP1 AE15 P_SSP_TX1P P_SSP_TX1P 20
USB_SS_TXN1 AF15 P_SSP_TX1N P_SSP_TX1N 20

U32_LAN

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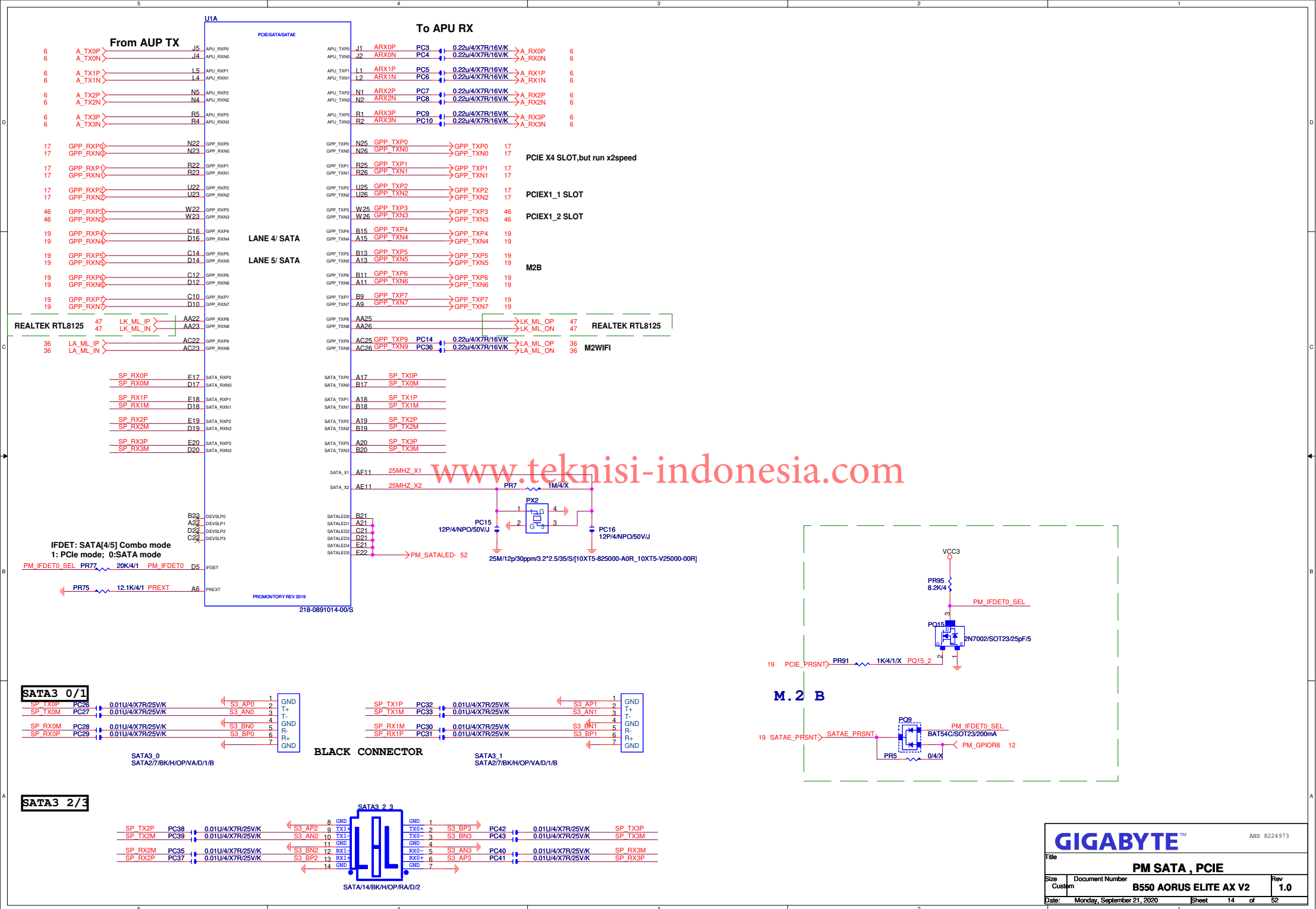
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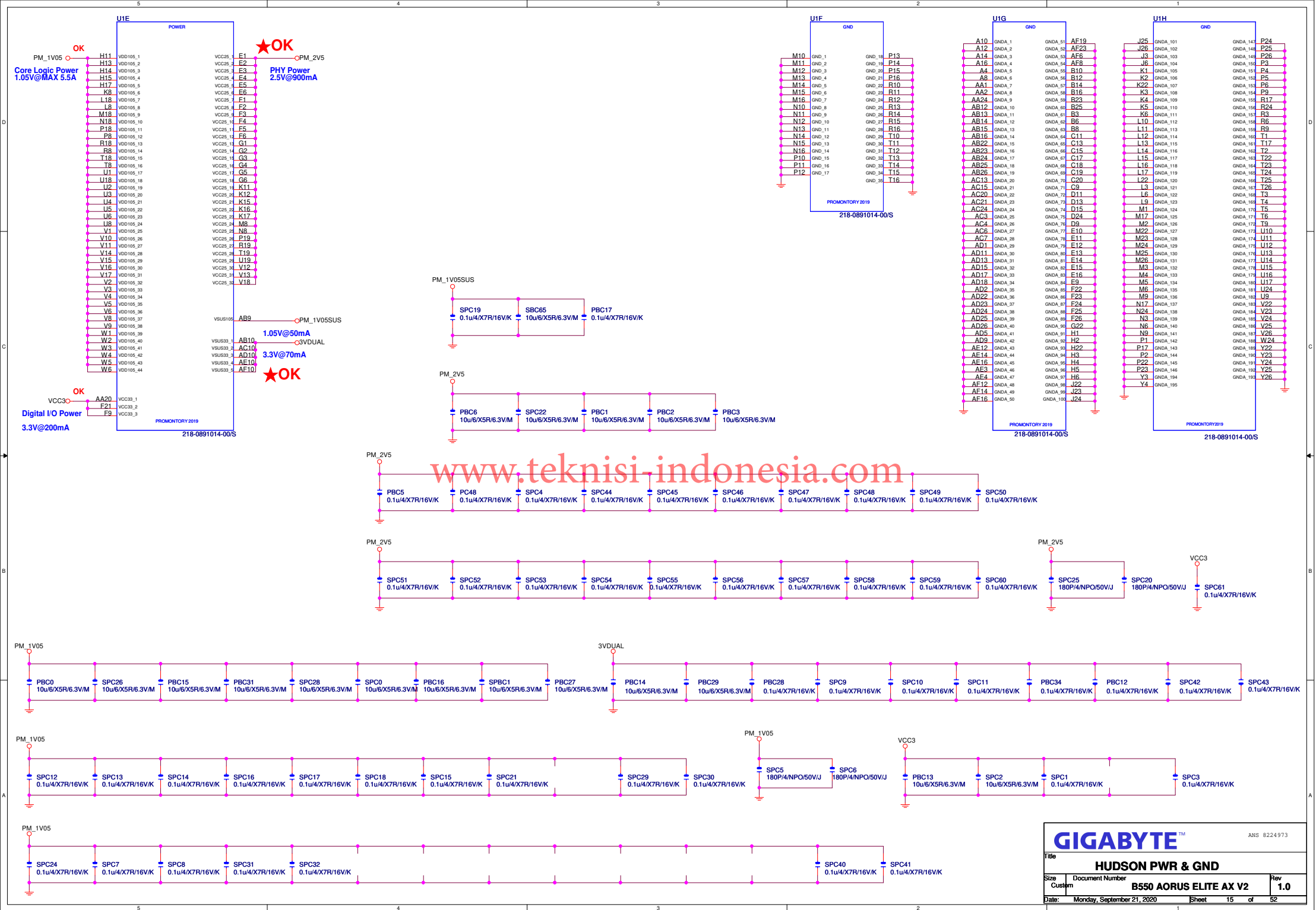
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Title PM USB

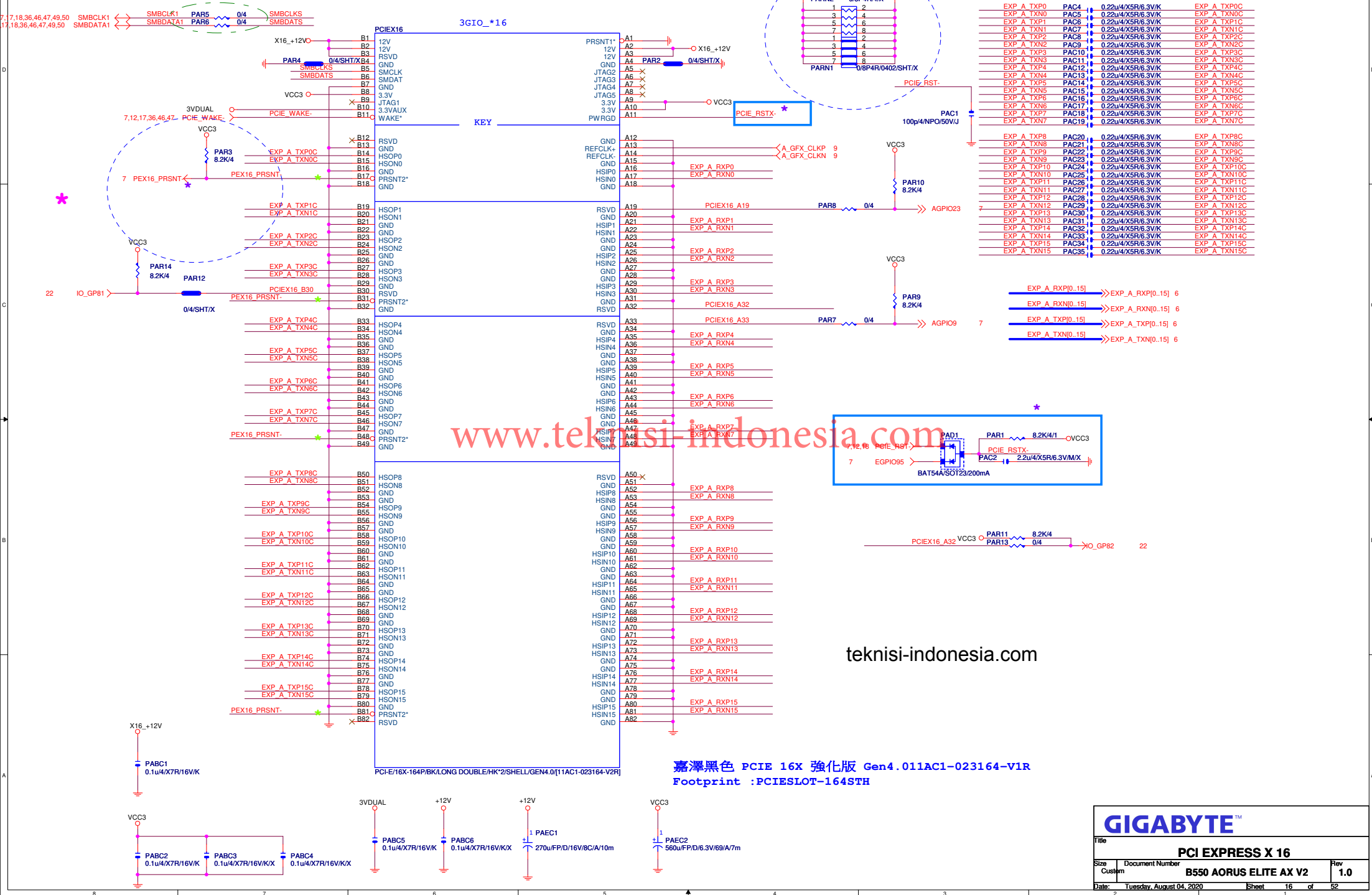
Size Custom Document Number B550 AORUS ELITE AX V2 Rev 1.0

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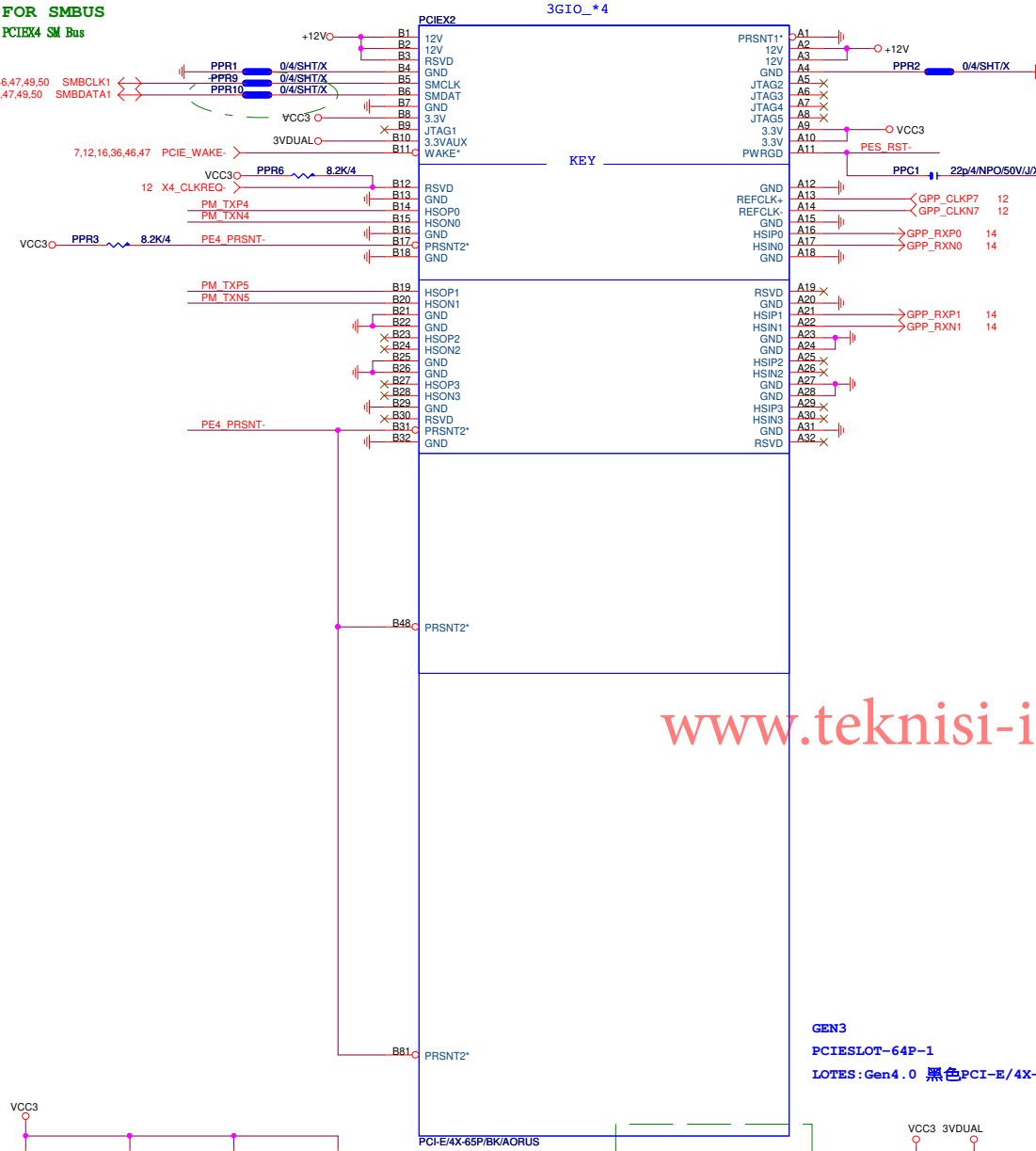




FOR SMBUS
PCIEX16不能short pad ,不上件

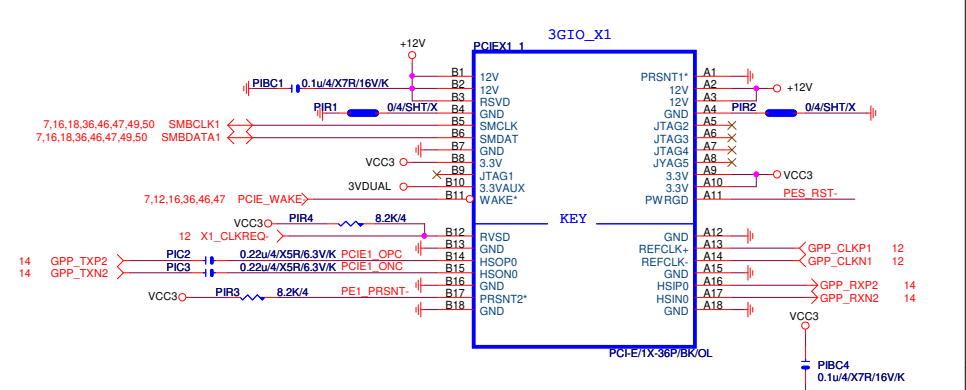
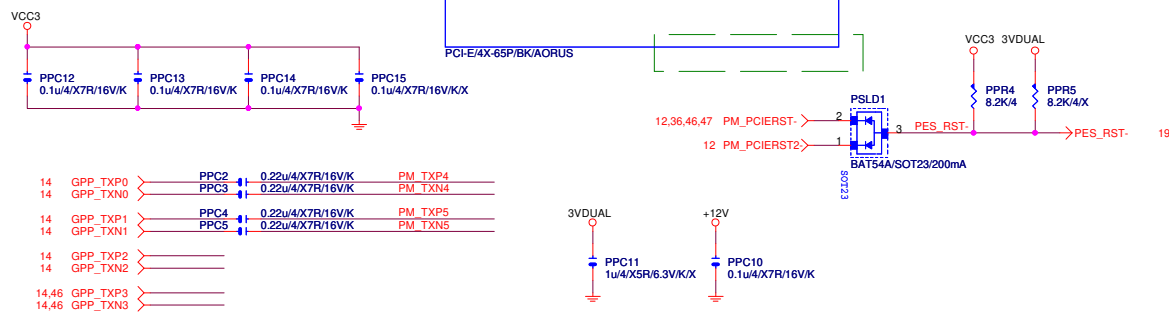


FOR SMBUS
PCIE4 SM Bus



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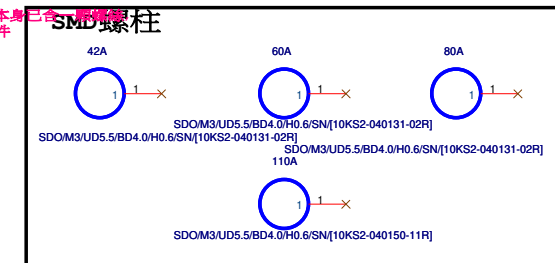
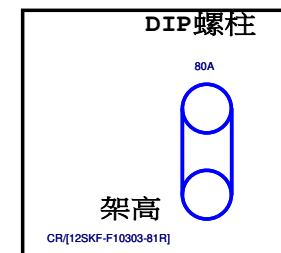
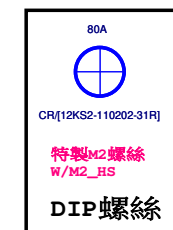
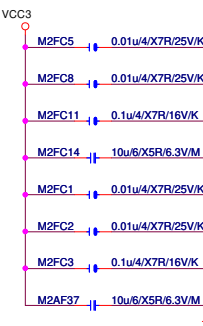
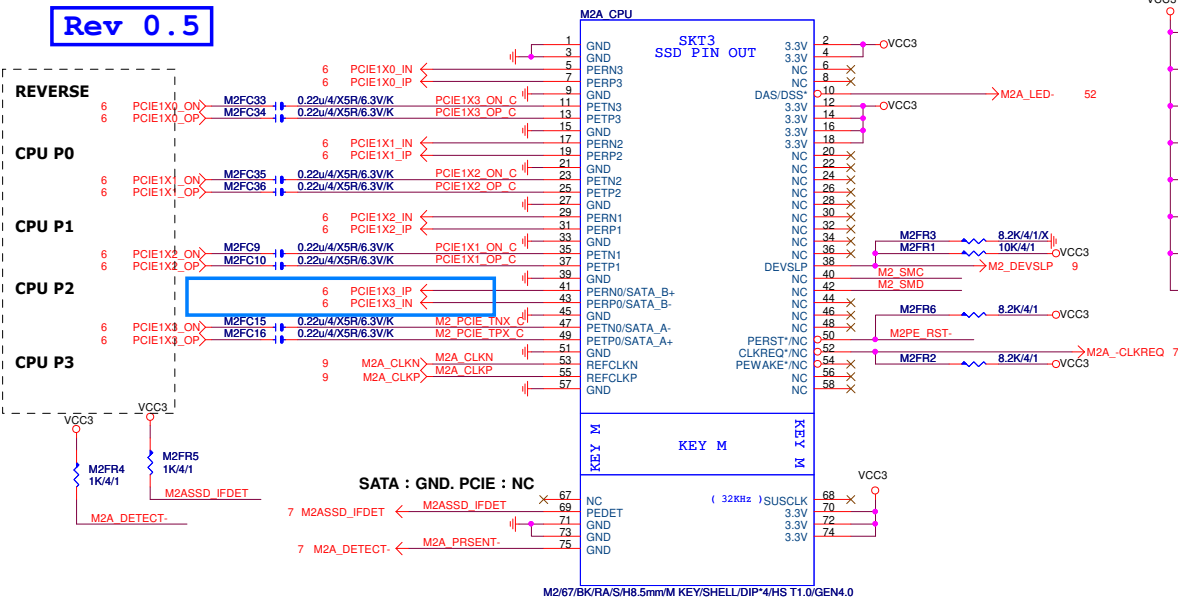
GEN3
PCIESLOT-64P-1
LOTES:Gen4.0 黑色PCI-E/4X-66P/BK/LONG DOUBLE :11AC1-023065-17R



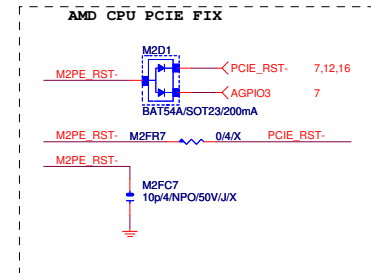
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Title PCIE X4, X1		
Size Custom	Document Number B550 AORUS ELITE AX V2	Rev 1.0
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Rev 0.5



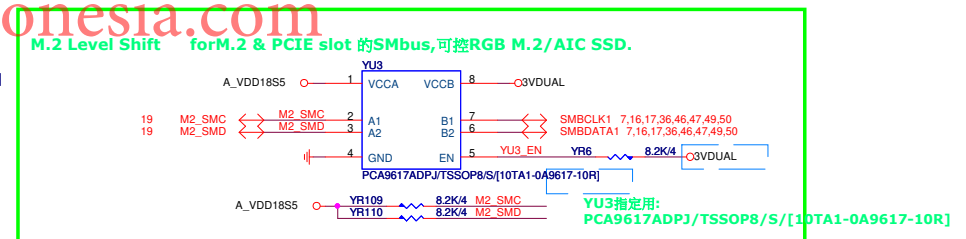
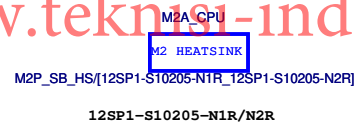
```
del M.2 slot heatsink
```

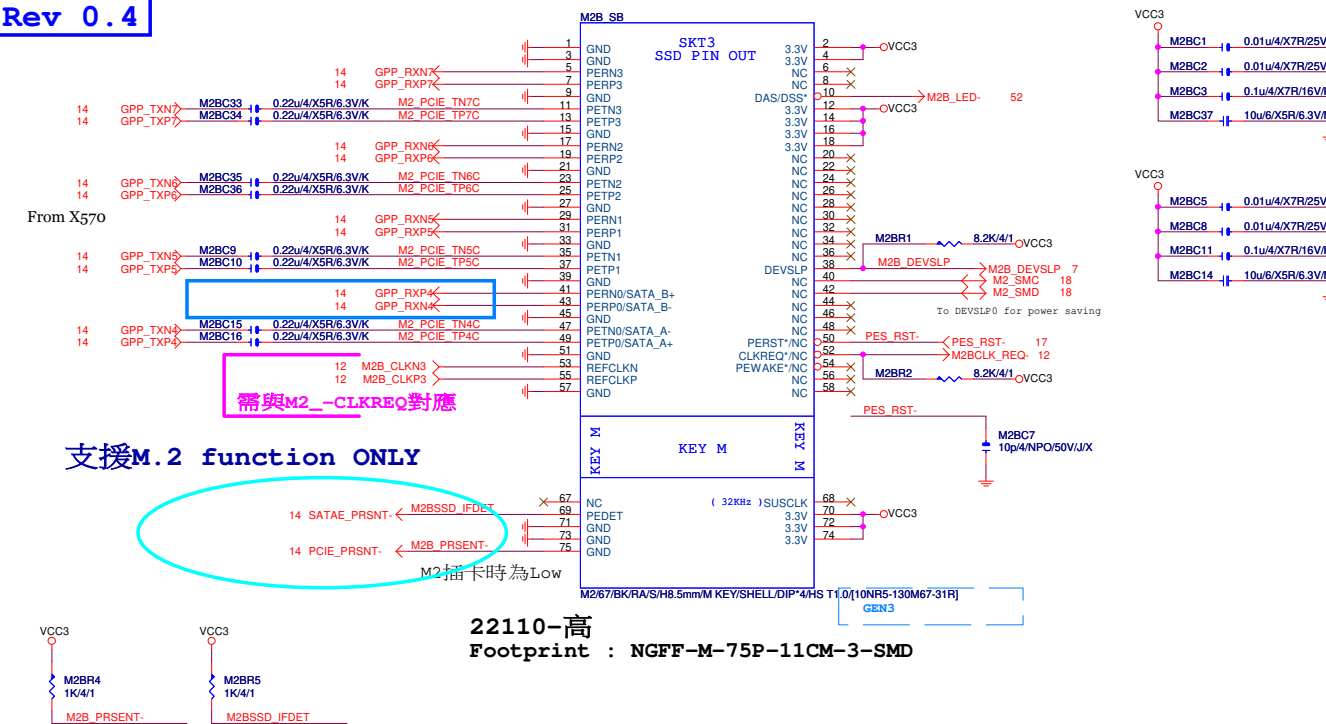


22110-高
Footprint : M2_110_H2MM8W

刪除SMD螺柱文字面 "A" ,不要show 出在PCB文字面上

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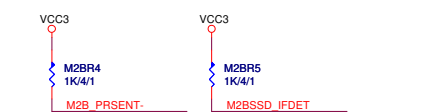




From X570

支援M.2 function ONLY

需與M2_-CLKREQ對應



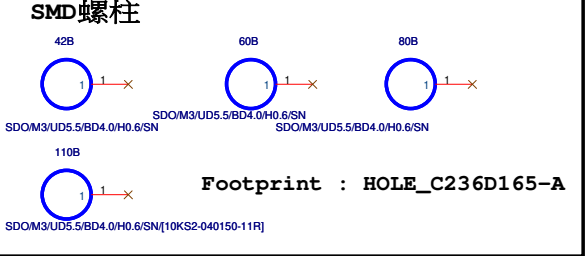
22110-高
Footprint : NGFF-M-75P-11CM-3-SMD

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刪除M2C_SOCKET & PU1



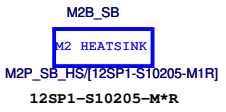
DIP螺絲



SMD螺柱

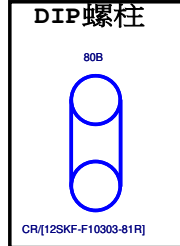
Footprint : HOLE_C236D165-A

刪除SMD螺柱文字面 "B" , 不要show 出在PCB文字面上



M2B_SB

M2P_SB_HS[12SP1-S10205-M1R]
12SP1-S10205-M*R



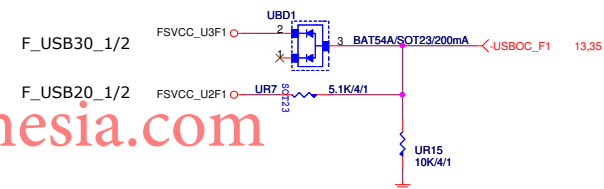
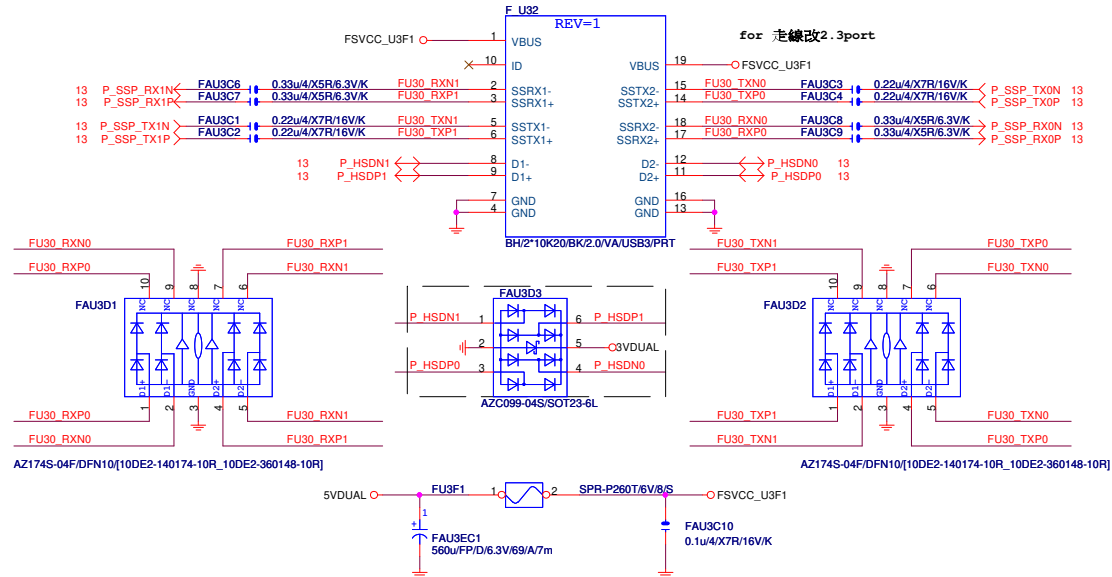
DIP螺柱

CR[12SKF-F10303-81R]

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Title					M.2 SLOT FROM PCH(B)					
Size	Custom	Document Number			B550 AORUS ELITE AX V2			Rev		1.0
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FRONT SIDE USB30



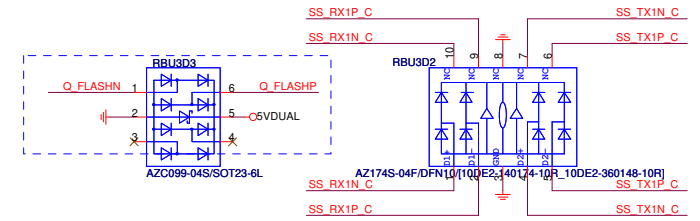
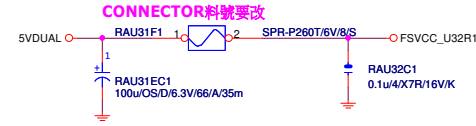
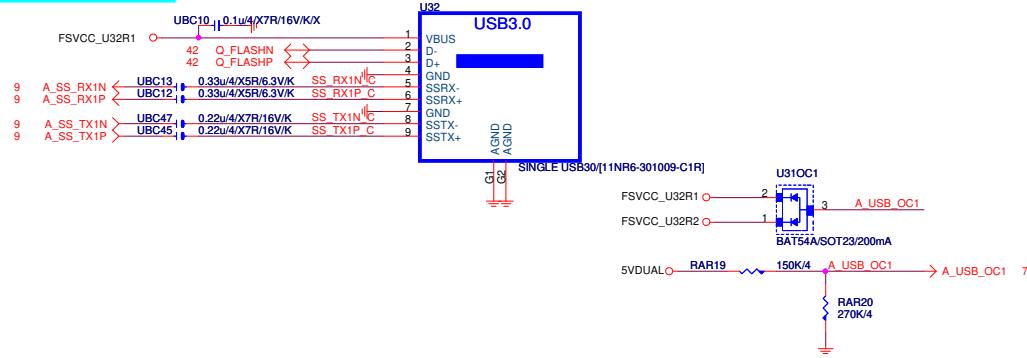
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Color markers can be changed by model

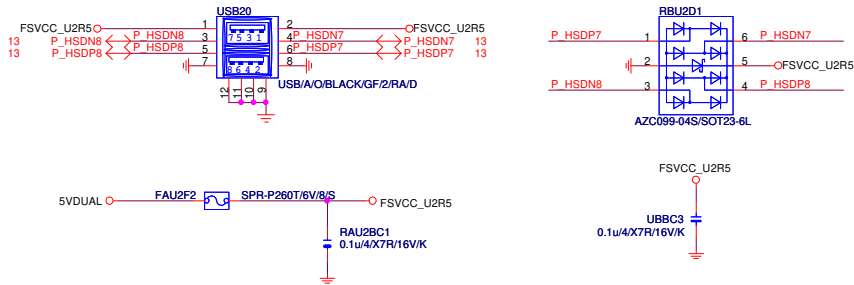
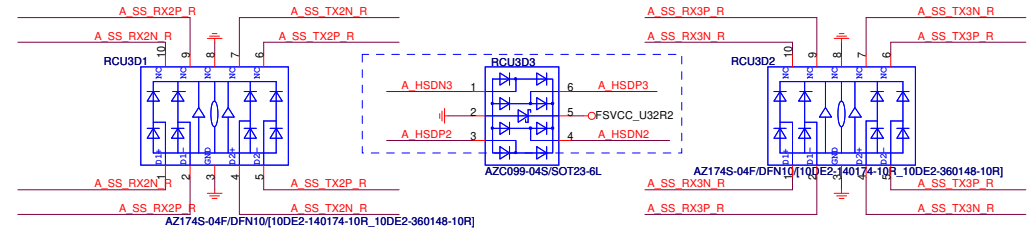
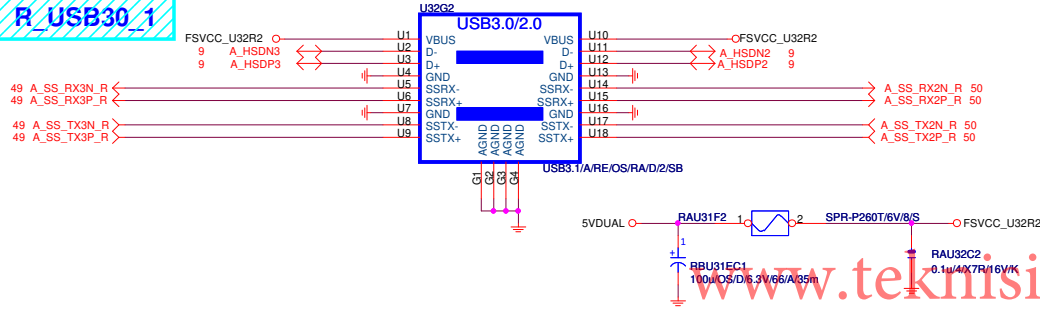
R_USB30_2

FROM PCH
USB30-SINGLE



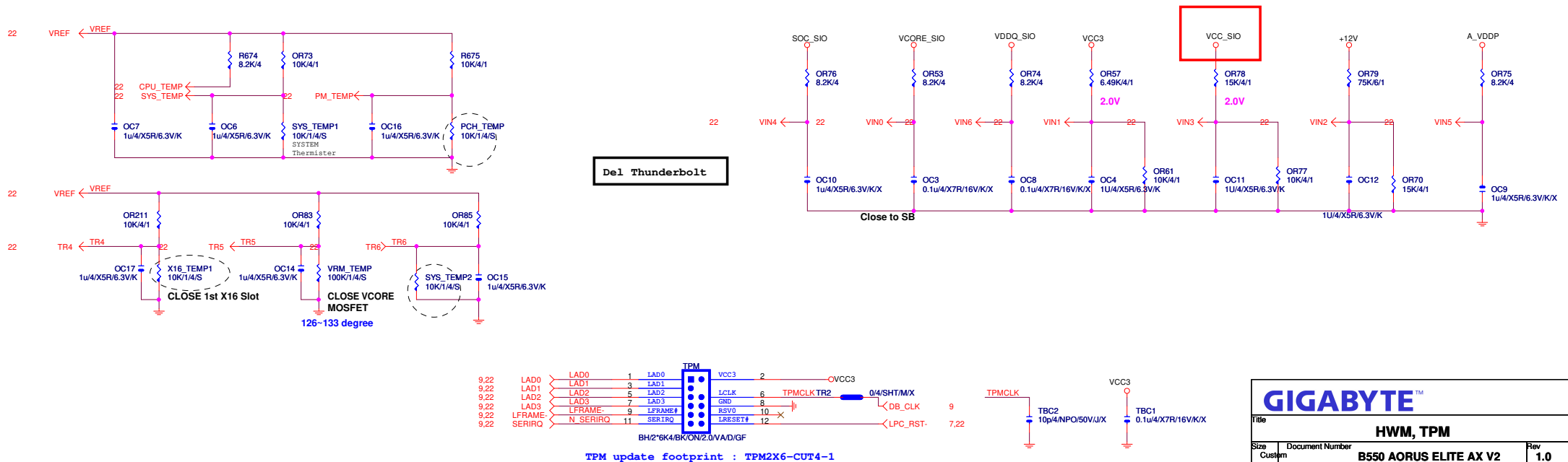
R_USB30_1

FROM CPU



删除clk

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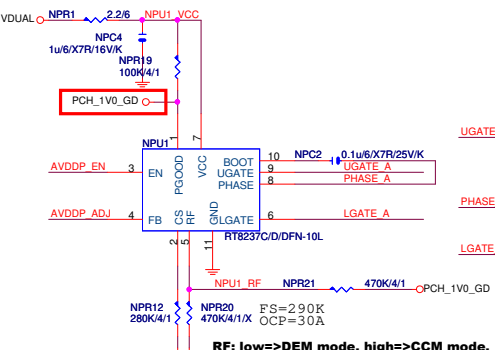


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Title			
HWM, TPM			
Size	Document Number	Rev	
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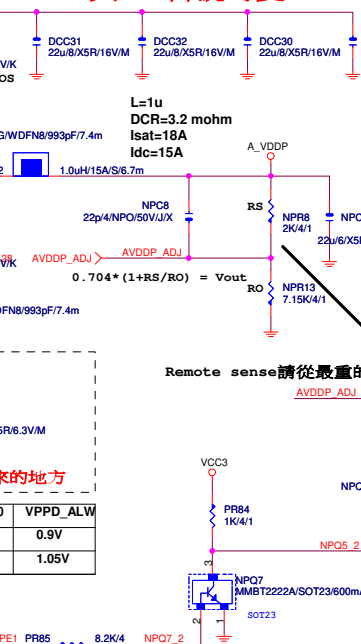
USB OC PROTECT

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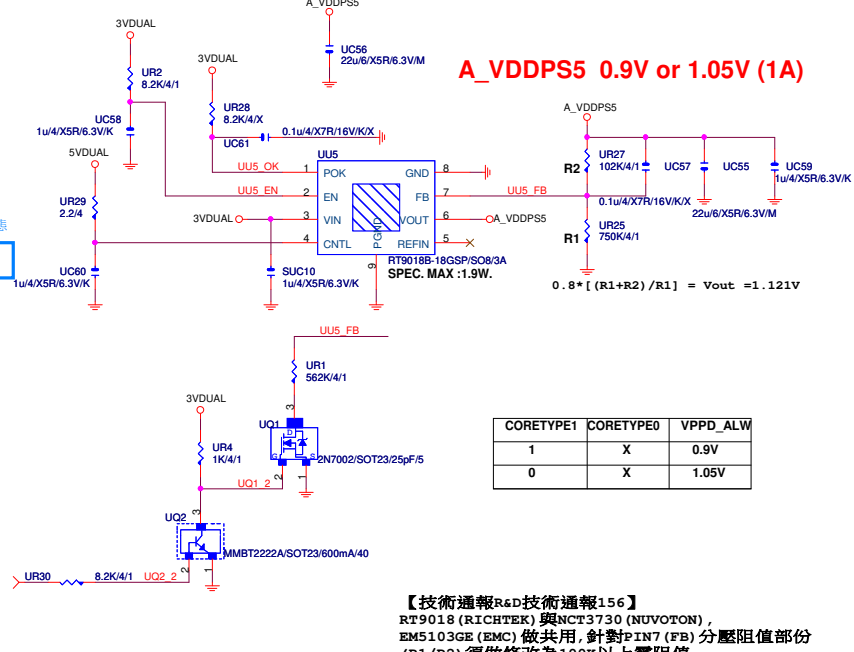
A VDDP



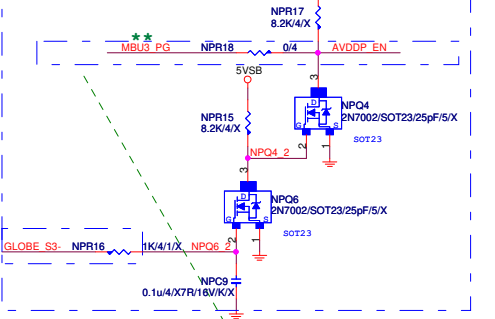
A_VDDP 0.9V or 1.05V



A_VDDPS5



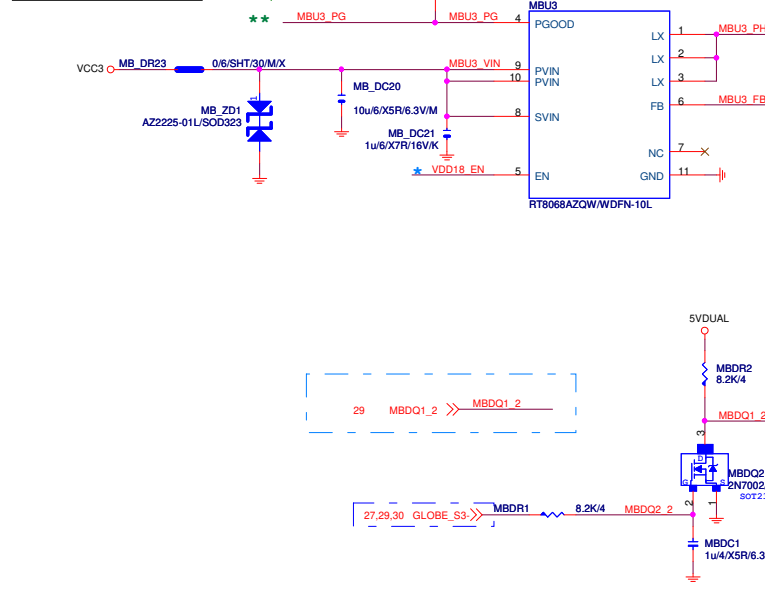
PWR_SEQ



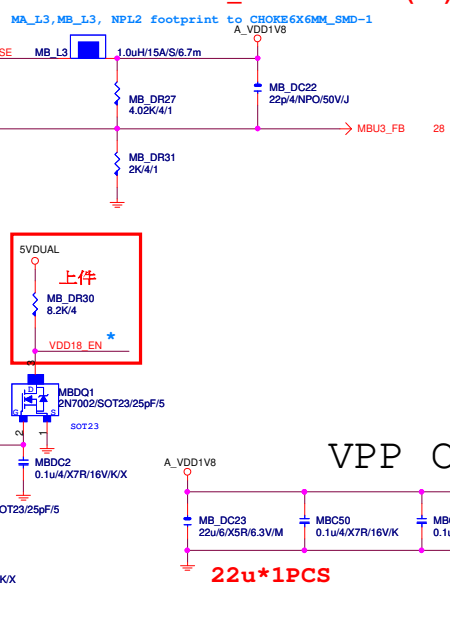
CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V

REV: 0.4

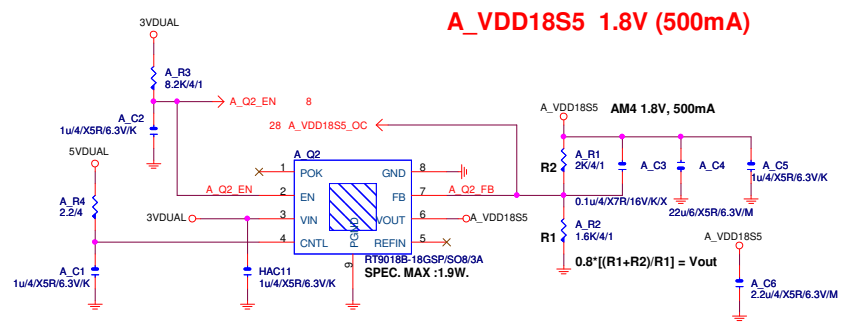
A_VDD1V8



A_VDD1V8 1.8V (2A)



A_VDD18S5

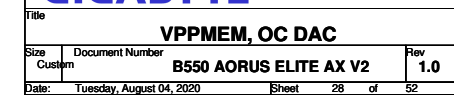


A_VDD18S5 1.8V (500mA)

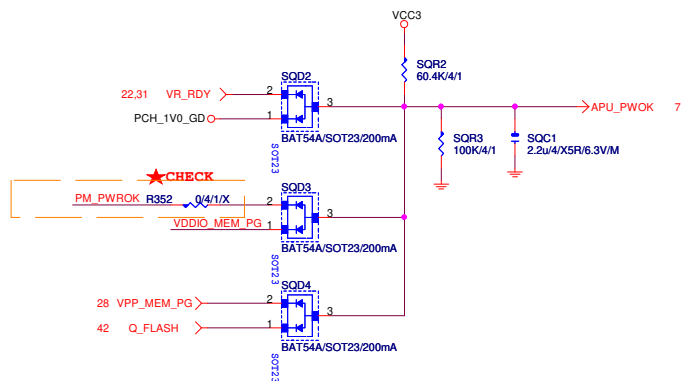
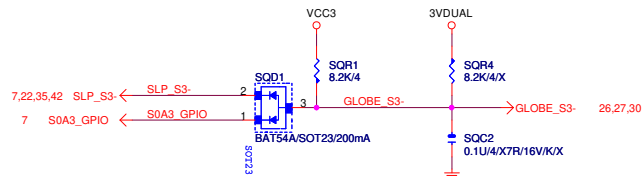
VDDCR SOC S5

S5_MUX: S0-->High, S5-->Low
H: VDDCR_SOC_S5 will track VCORE_SOC.
L: If VCORE_SOC < 0.775V (OR 0.85V), VDDCR_SOC_S5=0.775V.
If VCORE_SOC >= 0.775V (OR 0.85V), VDDCR_SOC_S5 will trace VCORE_SOC.

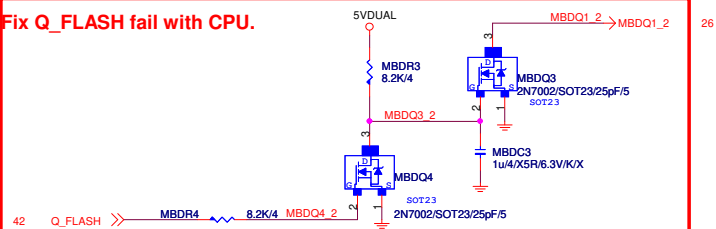
GIGABYTE™			
Title: A_VDDP/A_VDDPS5/A_VDD1V8/A_VDD18S5			
Size: Custom	Document Number: B550 AORUS ELITE AX V2	Rev: 1.0	
Date: Tuesday, August 04, 2020	Sheet: 26	of 52	



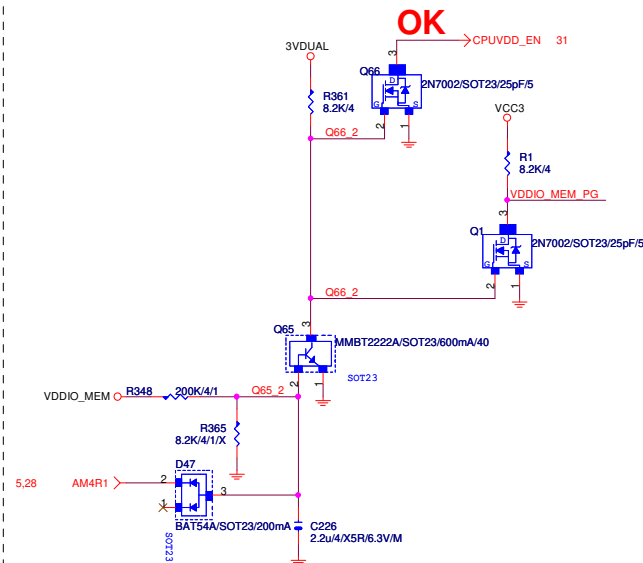
PWR SEQ



Fix Q_FLASH fail with CPU.

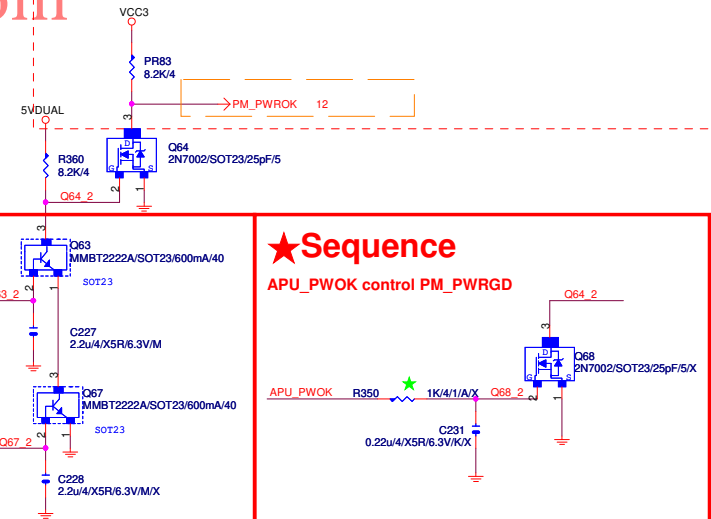


CPU PWR SEQ



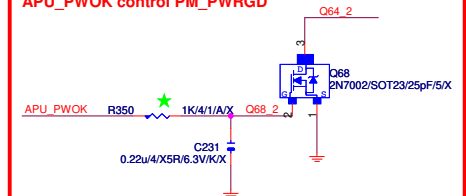
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PM	SWR	SEQ
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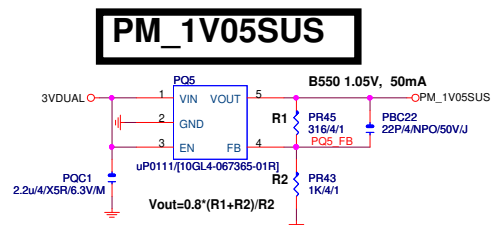
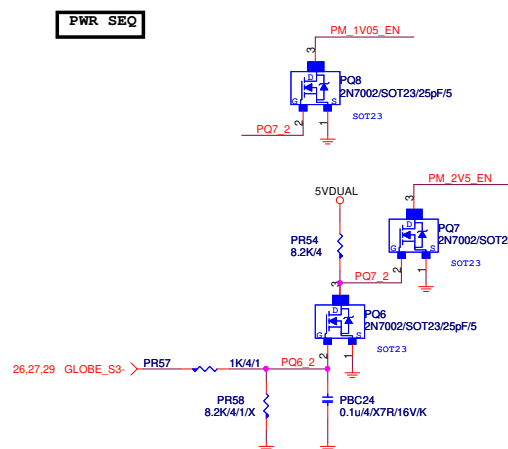
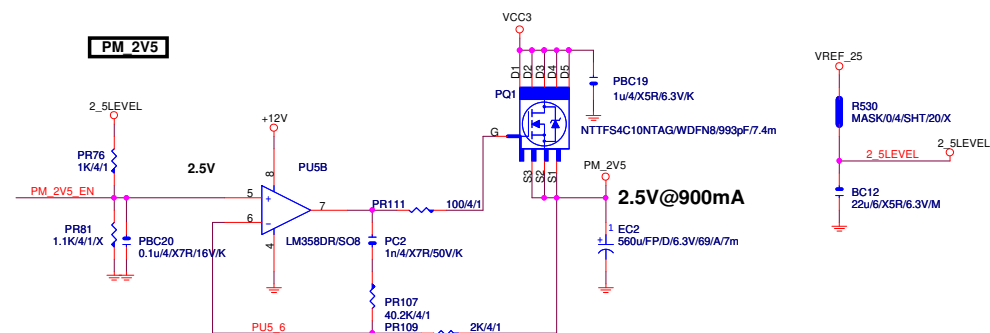
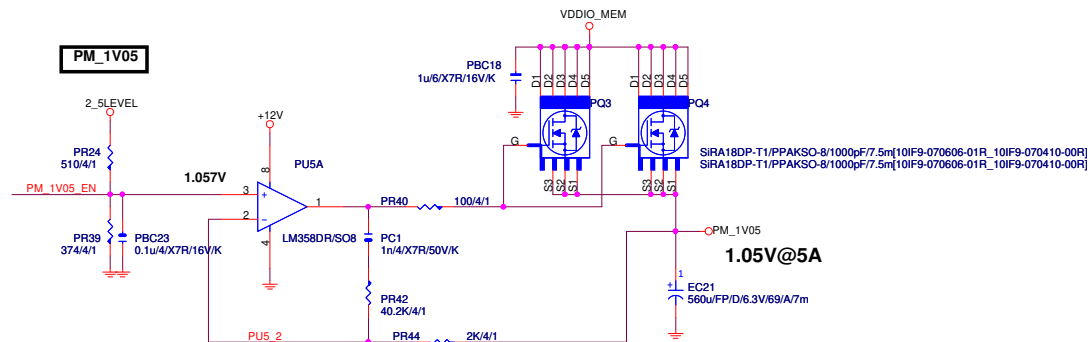
★ Sequence

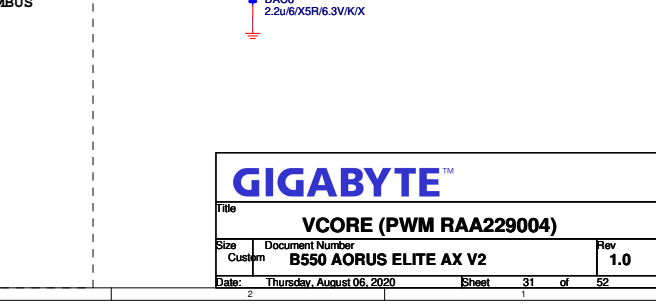
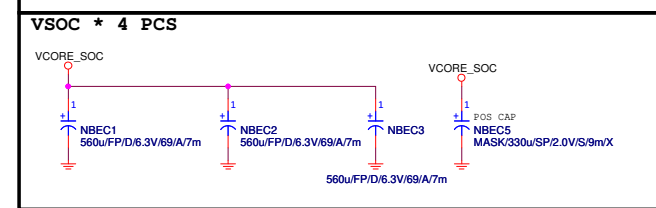
APU_PWOK control PM_PWRGD



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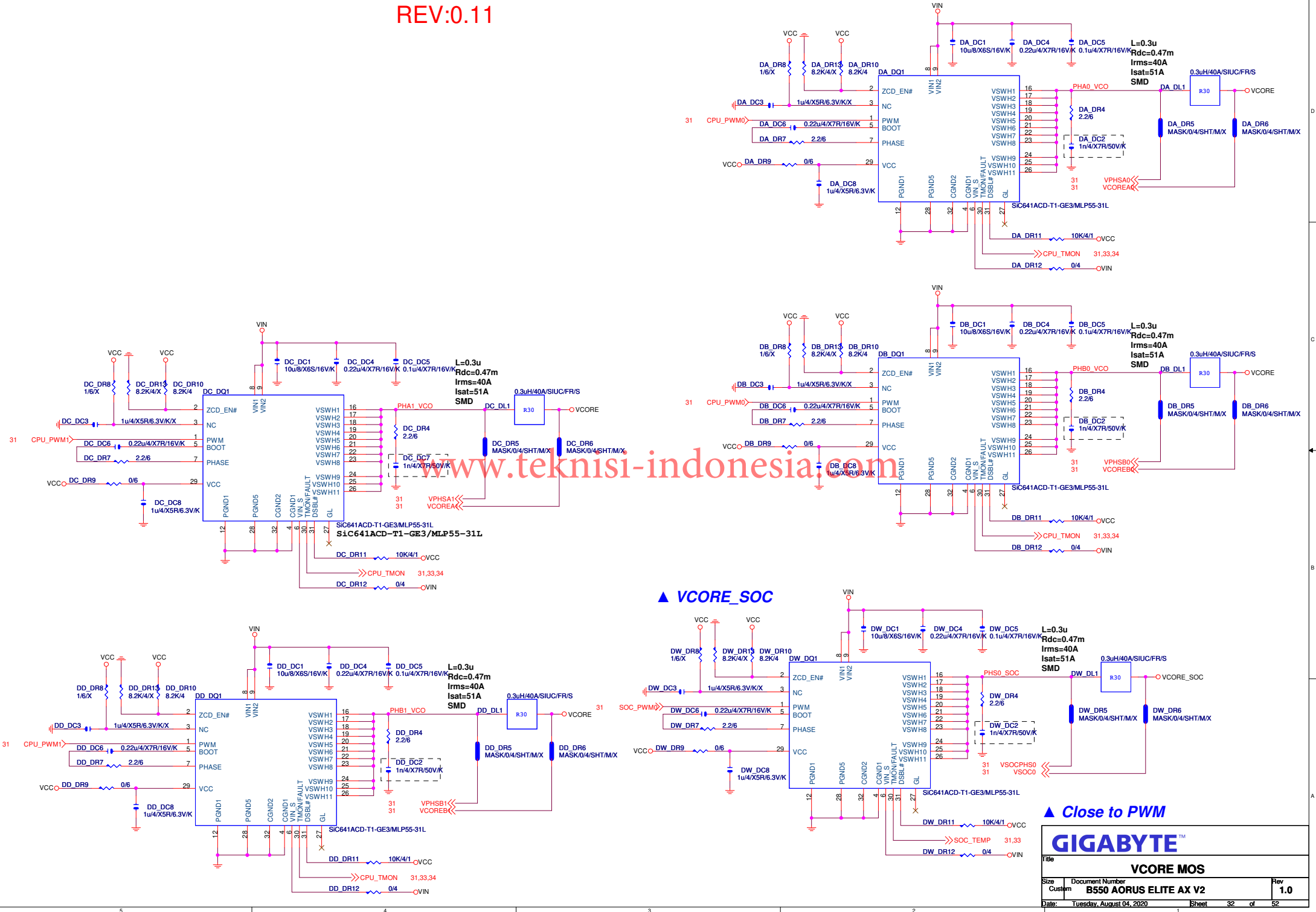
Title			
POWER SEQUENCE			
Size	Document Number	Rev	
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放置背板電感與電感之間

REV:0.11

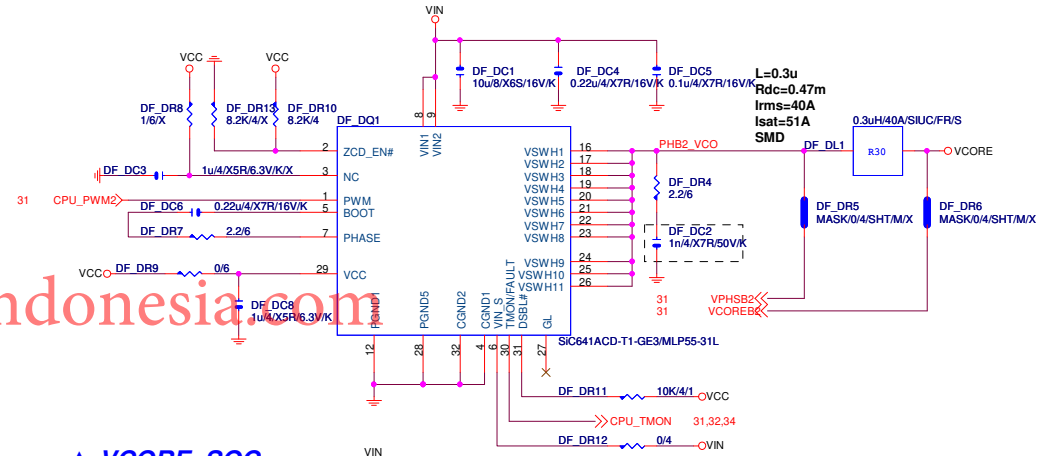
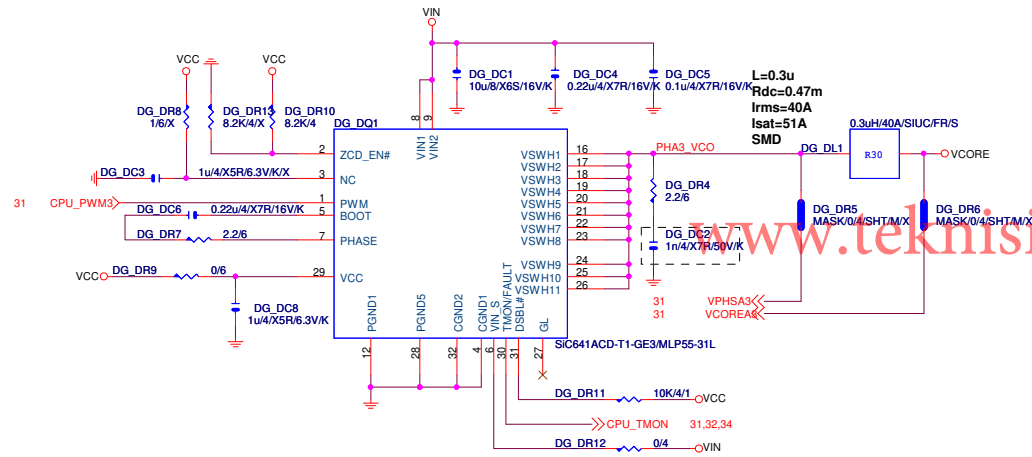
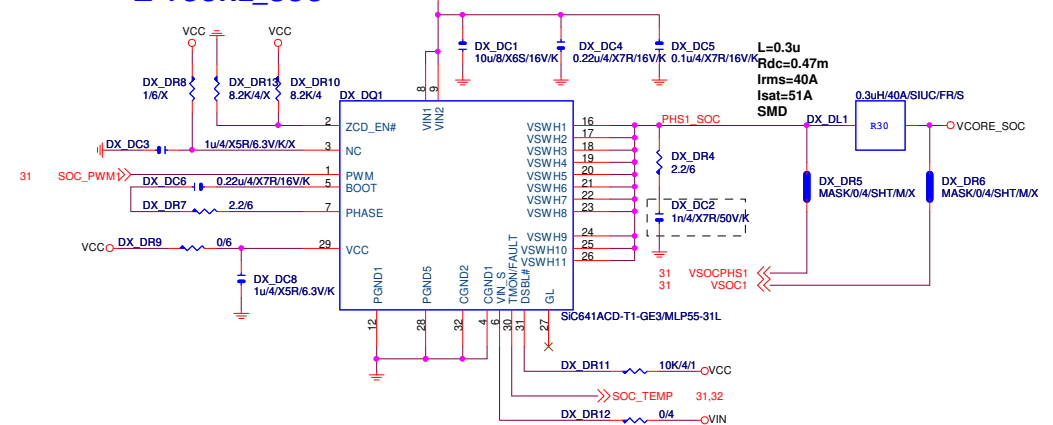


Close to PWM

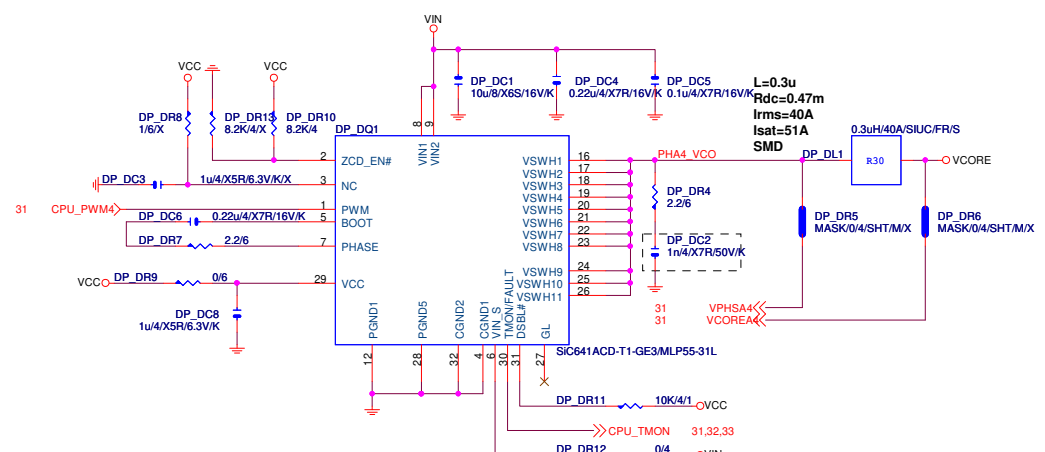
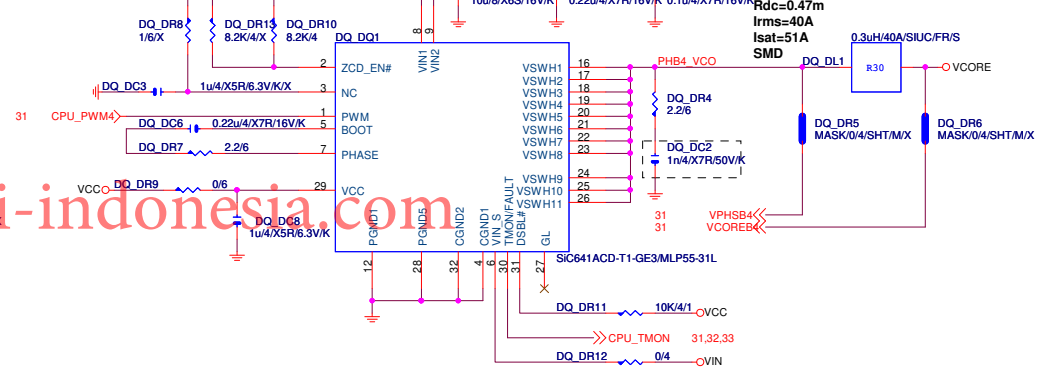
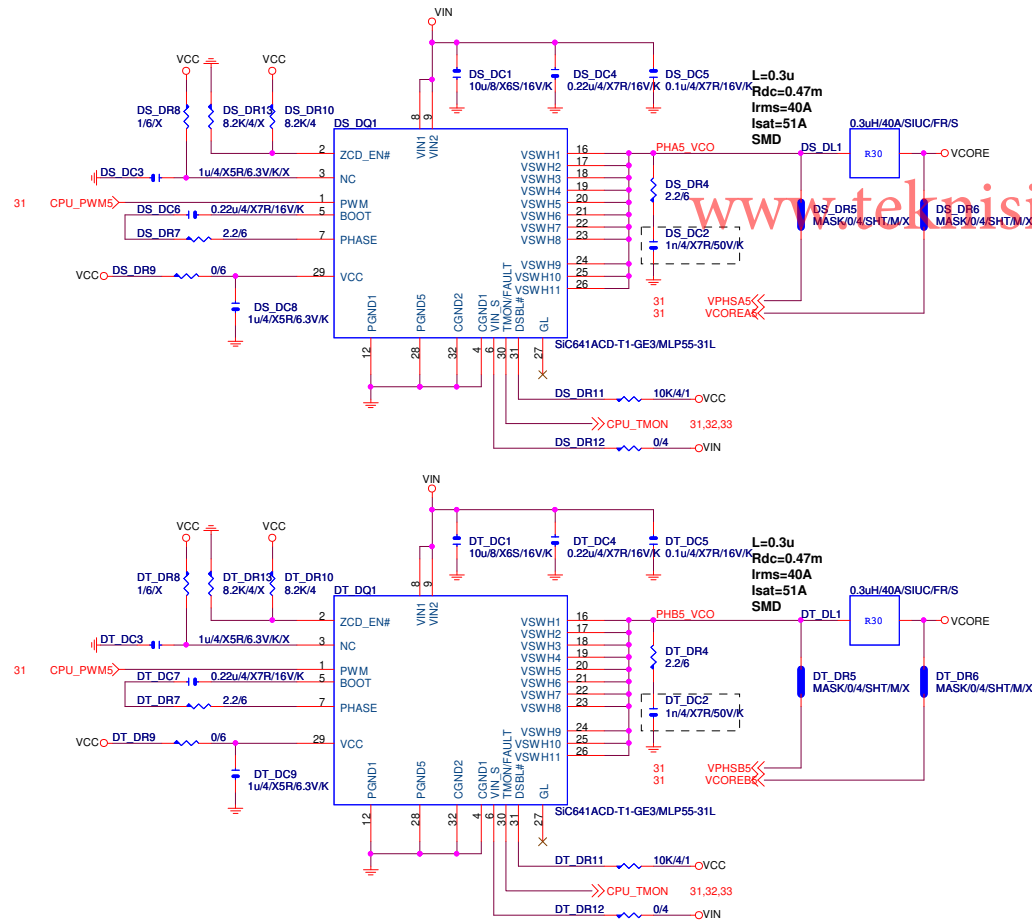
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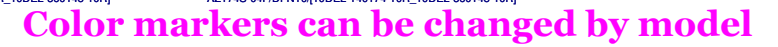
VCORE MOS

Title	VCORE MOS	
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[illegible]

REV:0.11

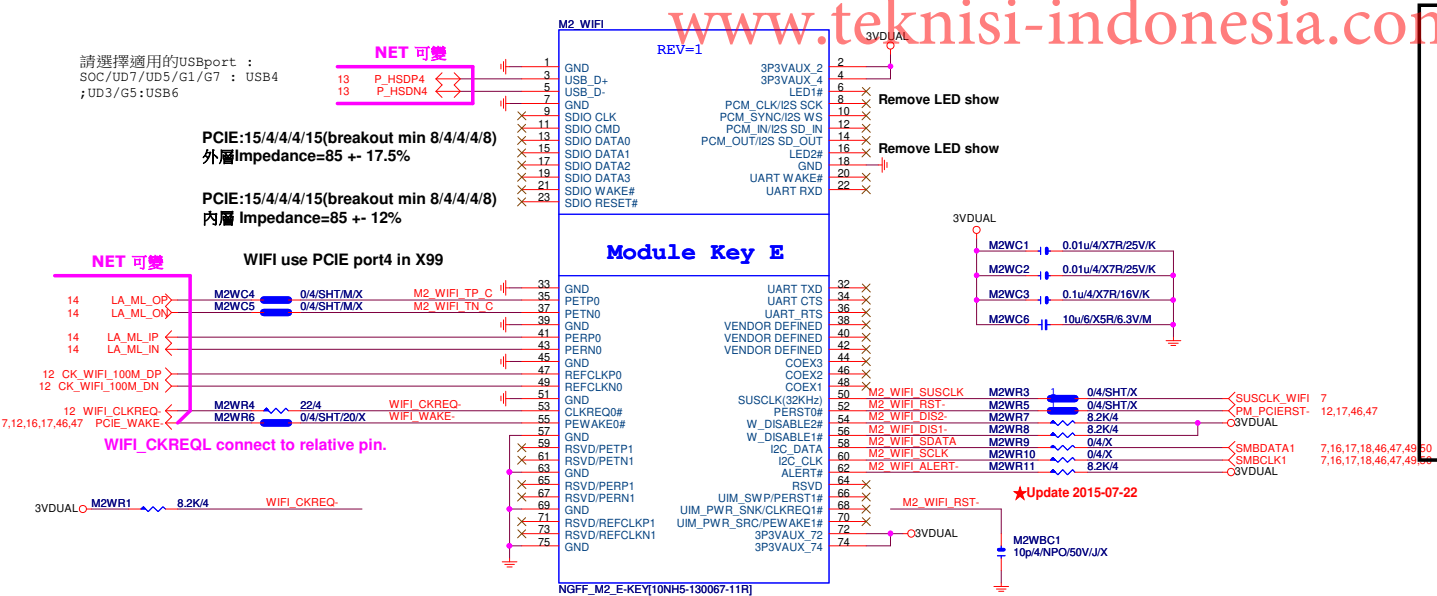




Title			
REAR TYPE C			
Size	Document Number	Rev	
Custom	B550 AORUS ELITE AX V2	1.0	
Date:	Tuesday, August 04, 2020	Sheet	35 of 63

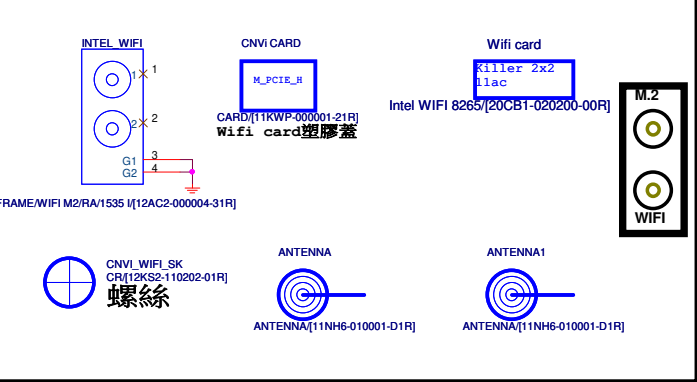
Rev: 0.2

FOR M.2 WIFI MODULE @ REAR PANEL



★Update 2015-02-11

一套WIFI MODULE包含外框+WIFI CARD+天線



Footprint Notice.

★Update 2015-07-22

★Footprint for
直立式 SMD:
WIFI-EKEY

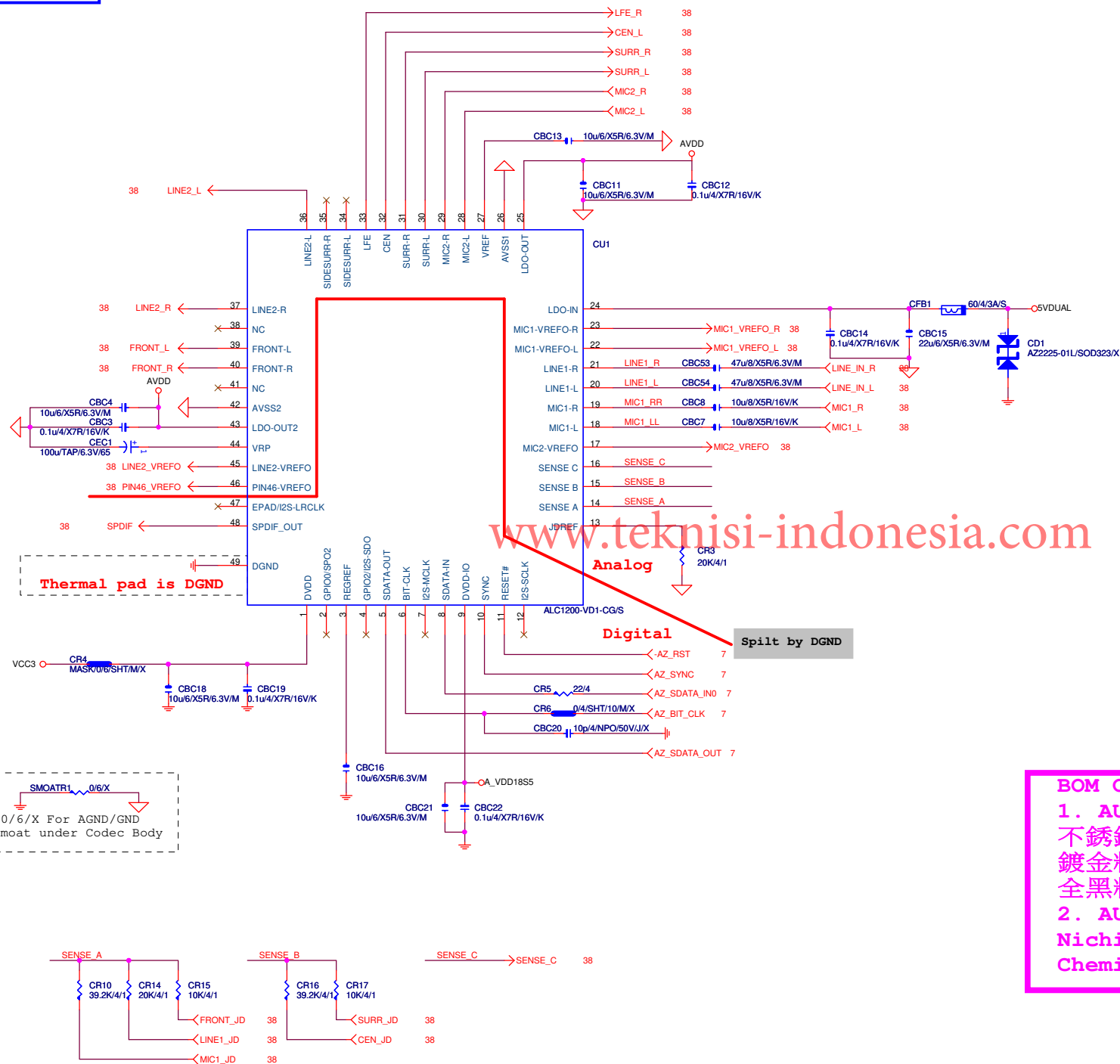
Footprint Notice.

★Update 2015-07-22

★Footprint for 橫式 SMD:
NGFF-E-75P-2

GIGABYTE™

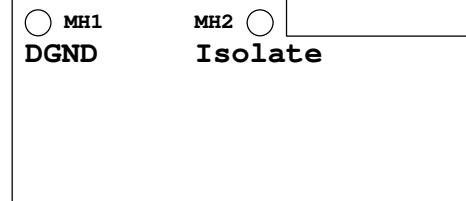
Title					
M.2, F TYPE C					
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LAYOUT注意: 螺絲孔下GND方式

1. MH1下DGND

2. MH2一律改為Isolate

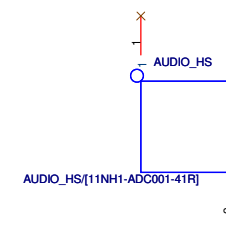


LAYOUT注意: 是否要加?

AGND切割線



音效區域印刷



BOM OPTION :

1. AUDIO CONNECT

不銹鋼料號: 11NR6-403025-A3R

鍍金料號: 11NR6-403025-92R

全黑料號: 11NR6-403025-B1R

2. AUDIO CAP

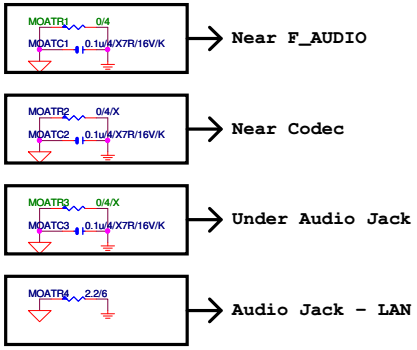
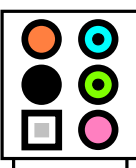
Nichicon MW音效電容 : 100u/TAP/6.3V/65

Chemicon音效電容 : 100uF/TAP/10V/6*5

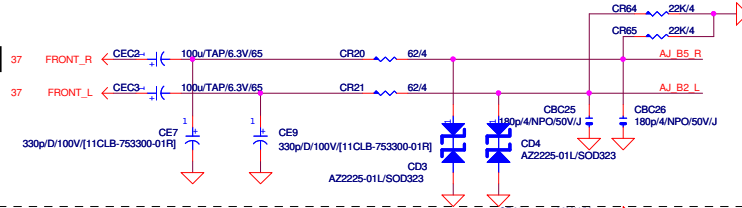
Gigabyte Technology

Title			ALC1220
Size	Document Number	Rev	
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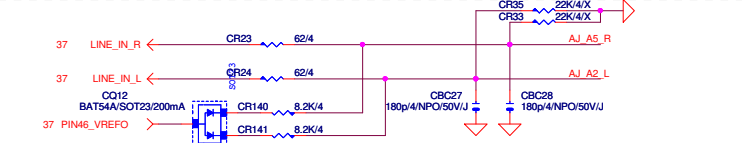
AZALIA JACK



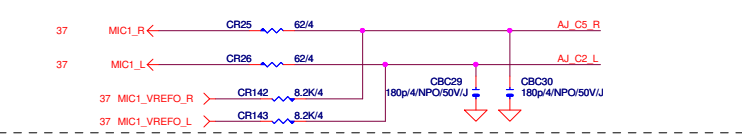
LINE-OUT



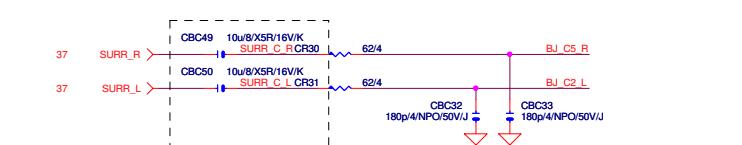
LINE-IN



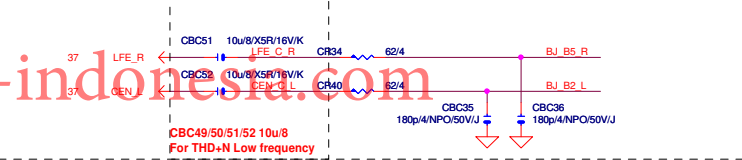
MIC-IN



SURROUND



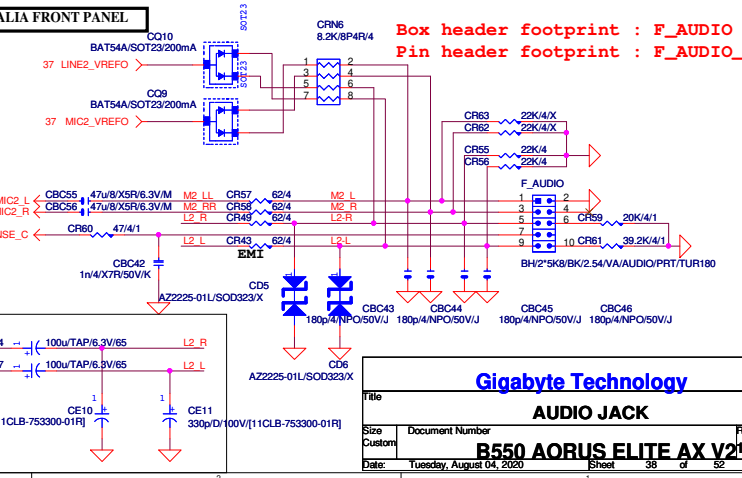
CEN/LFE



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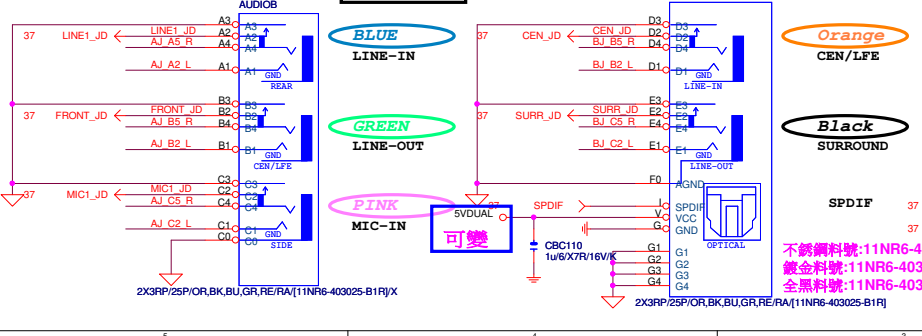
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AZALIA FRONT PANEL



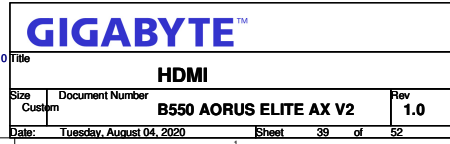
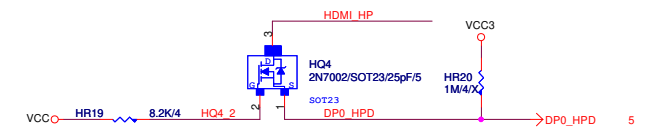
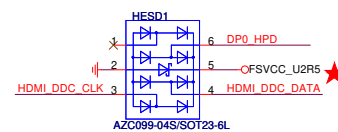
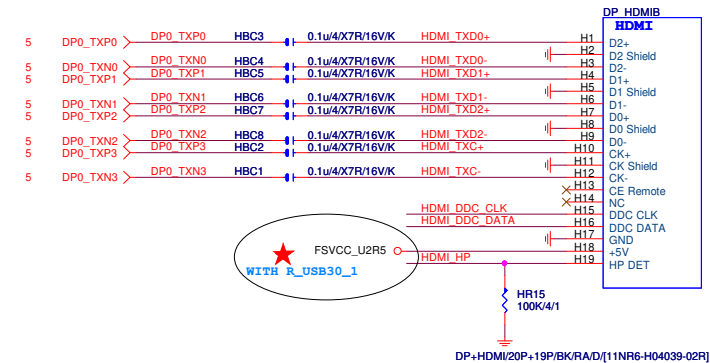
Box header footprint : F_AUDIO
Pin header footprint : F_AUDIO_S

AZALIA JACK

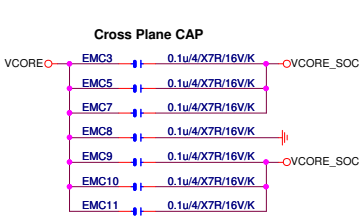
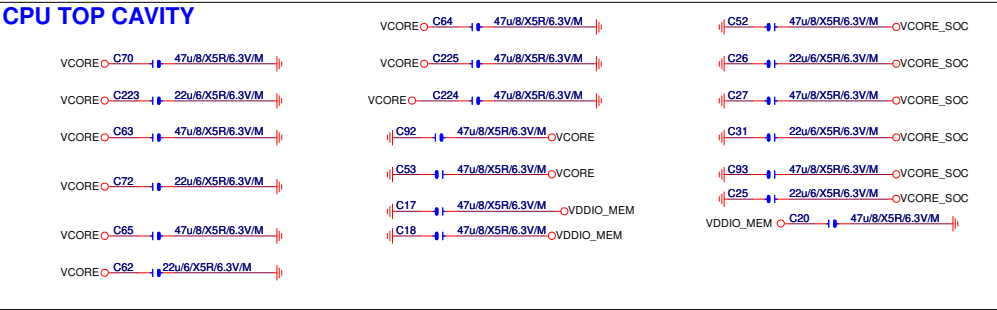


不銹鋼料號:11NR6-403025-A3R
鍍金料號:11NR6-403025-92R
全黑料號:11NR6-403025-B1R

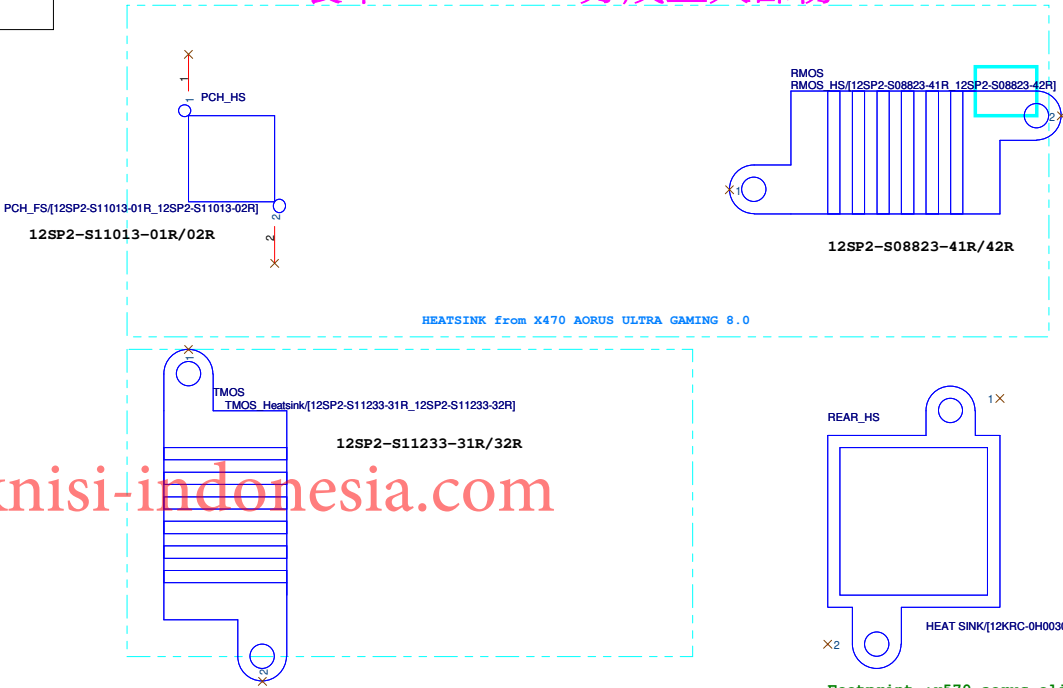
Gigabyte Technology		
AUDIO JACK		
File	Document Number	Rev
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CPU TOP CAVITY



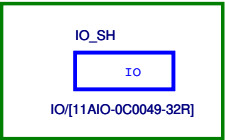
裝甲HEATSINK 分成五大部份

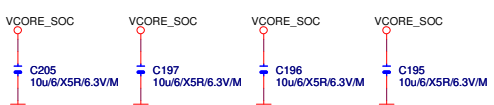
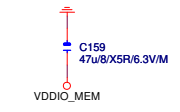
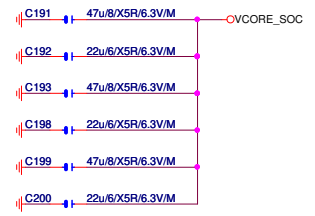
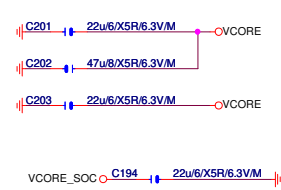
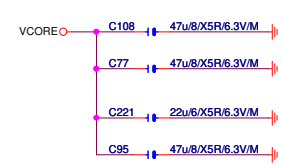
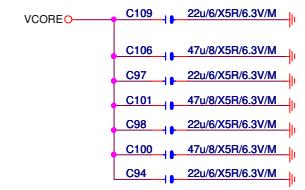
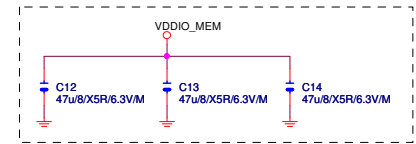
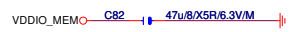
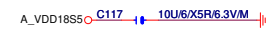
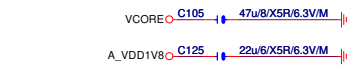
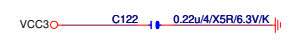
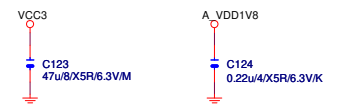
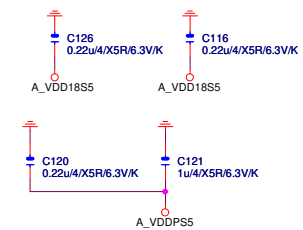
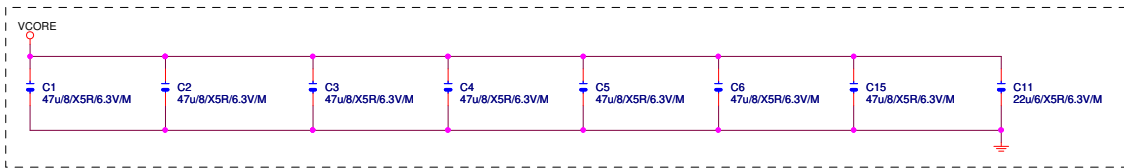


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Footprint :x570_aorus_elite_cover
PN: ?
Rear IO (裝甲不需透光, 正下方不需LED發光)

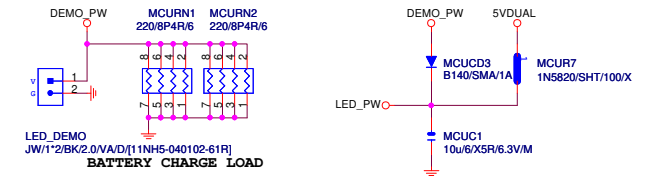
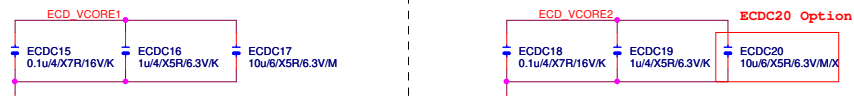
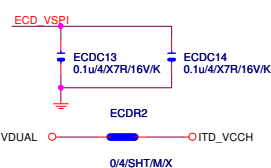
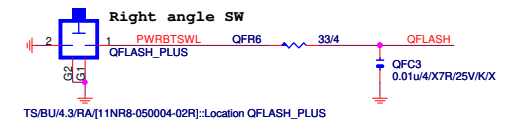
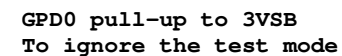
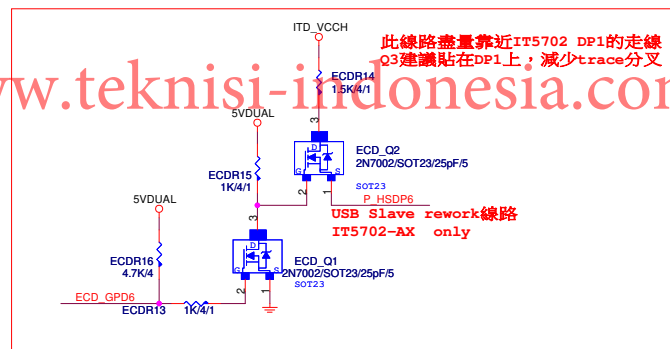
一體式IO料號
Z390 GAMING SLI?11AIO-0C0014-02R
Z390 GAMING X?11AIO-0C0015-02R
Z370 GAMING X?11AIO-0C0015-04R



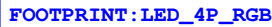


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Title			
BOTTOM			
Size	Document Number	Rev	
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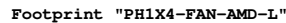


FOR 裝甲高亮度 正發光 LED*2 (位置在正板, 依據裝甲設計擺放)



第三區 LED CONTROL

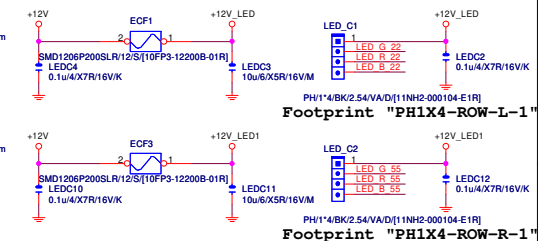
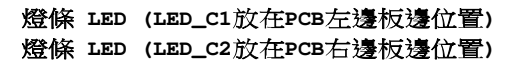
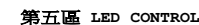
燈條 LED (LED_CPU放在CPU附近位置)



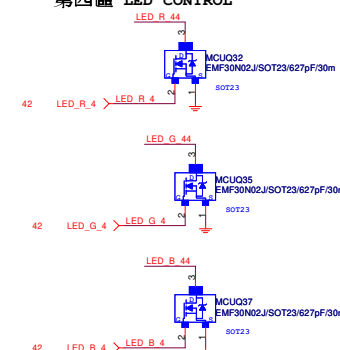
FOR AUDIO 背板正發光 LED*10 C_3LED1~10)



第二區 LED CONTROL

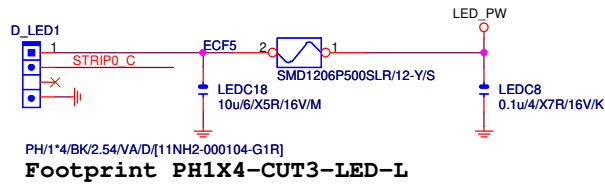


第四區 LED CONTROL



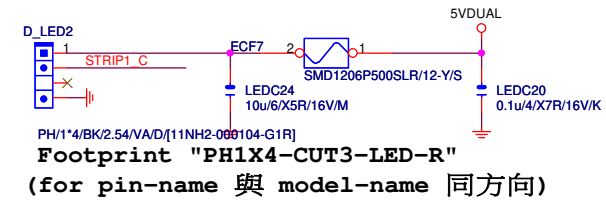
第六區 LED (靠近左上板邊位置)

Digital LED Strip1

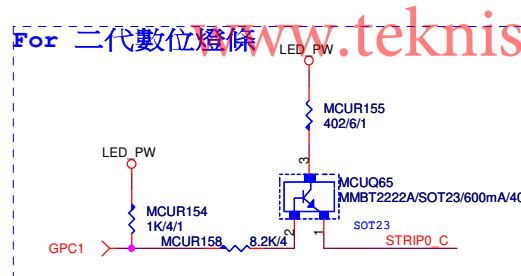
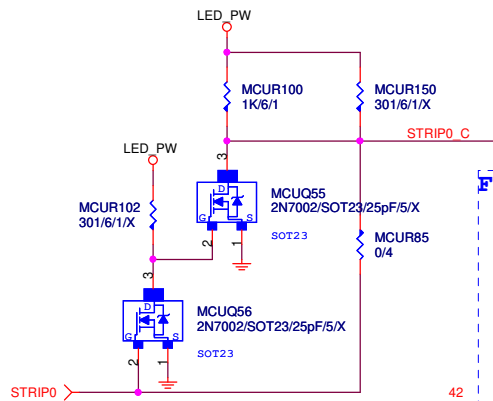


第七區 (靠近右下CPU板邊位置)

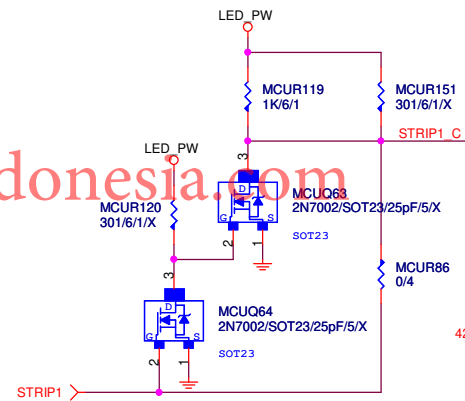
Digital LED Strip2



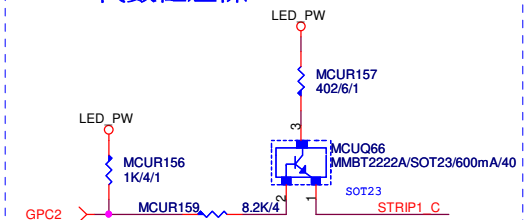
燈條 Level shift



燈條 Level shift



For 二代數位燈條

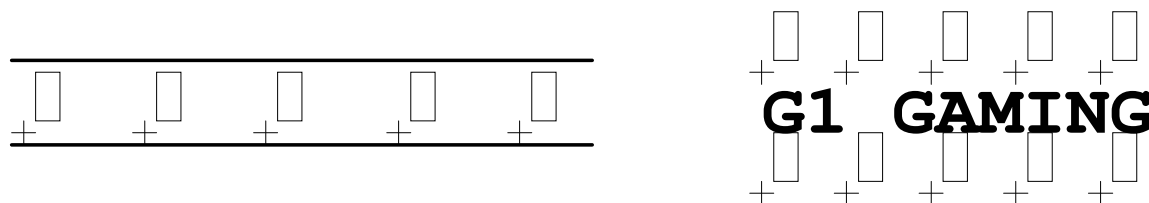


GIGABYTE™			
Title			
D_LED			
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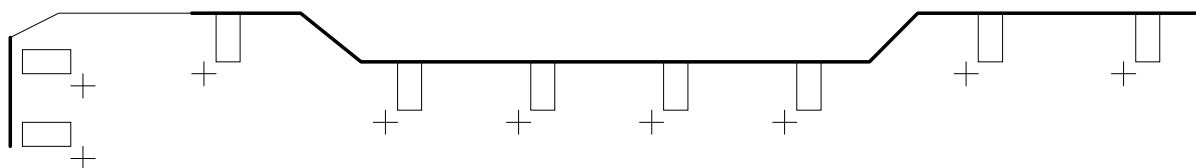
RGB LED LAYOUT 注意事項：

1. Debug LED (各LED依CPU/DRAM/VGA/BOOT個別位置擺放)
2. 背板 RGB LED 方向整板請統一如下
(整板正極可統一朝下或朝上)
3. 正板 RGB LED 統一方向即可
4. MCU_PW & MCU_PW33電源一律走20mils
5. ECF1,ECF2,ECF3,ECF5 兩端電源走80mils或用鋪銅方式加粗
6. MCU LED 出pin的走線4mils,如:LED_R_1,LED_G_1,LED_B_1
7. LED RGBW rule :W/S=10/5 mils 如:LED_R_11,LED_G_11,LED_B_11..
(包含從晶體到排阻到LED的net)
8. Digital LED NET rule W/S=4/8 mils
GPD0_SDA_B,GPD0_SDA_BB,GPD0_SDA_C,GPD0_SDA_CC

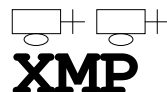
PCB板邊透光model name鏤空+背面 RGB LED



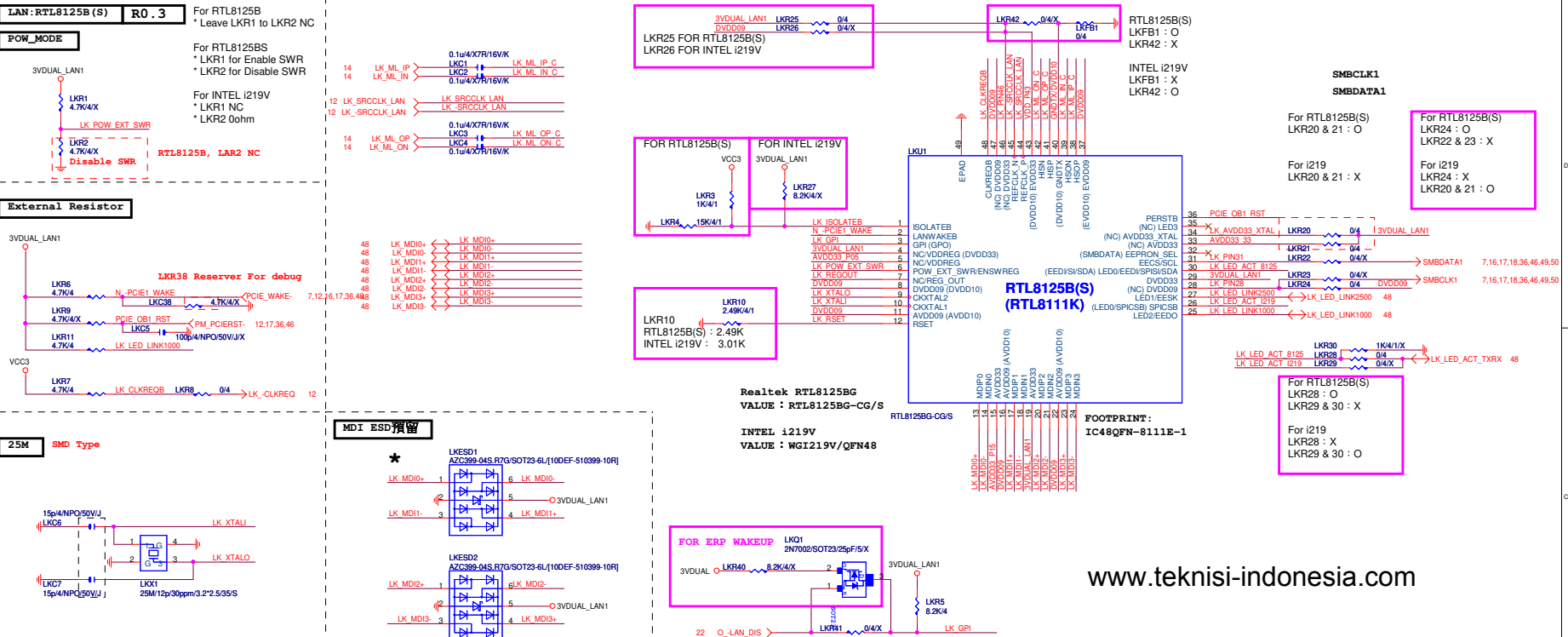
Audio Ground切割線+背面 RGB LED



"XMP"字樣鏤空+背面 RGB測發光 LED



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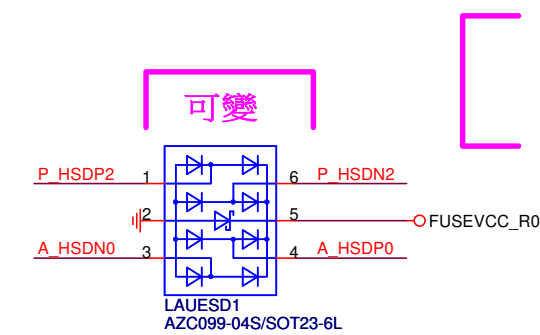


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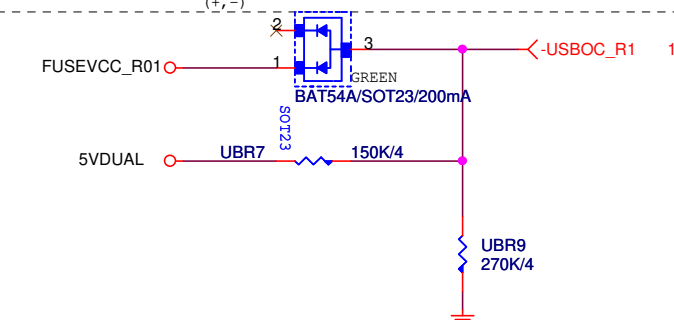
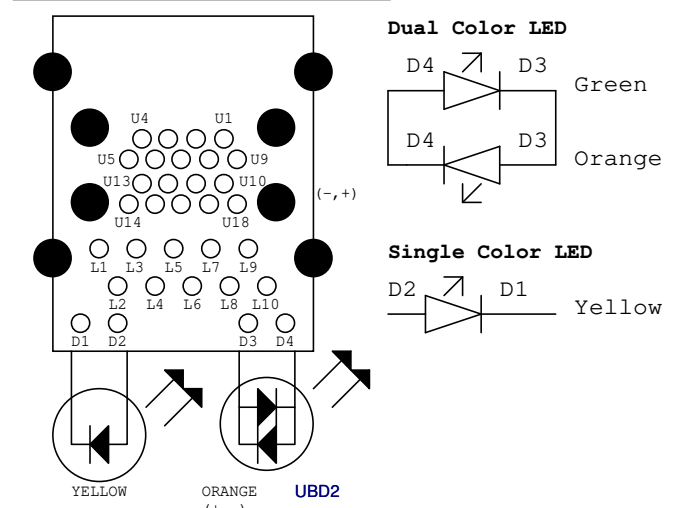
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USB_LAN CONNECTOR R0.1

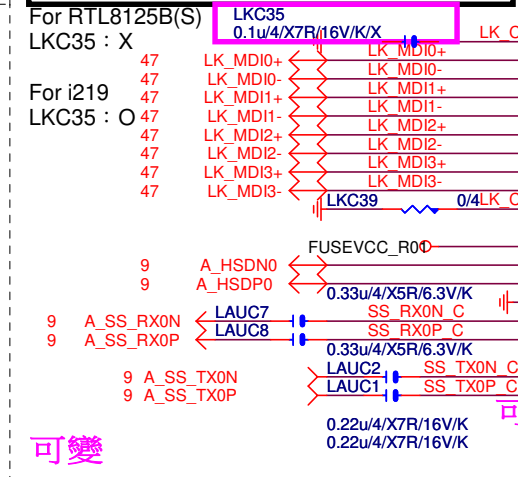
RMA ESD PROTECT note:可變更USB NAME



USB30_LAN LAYOUT示意圖

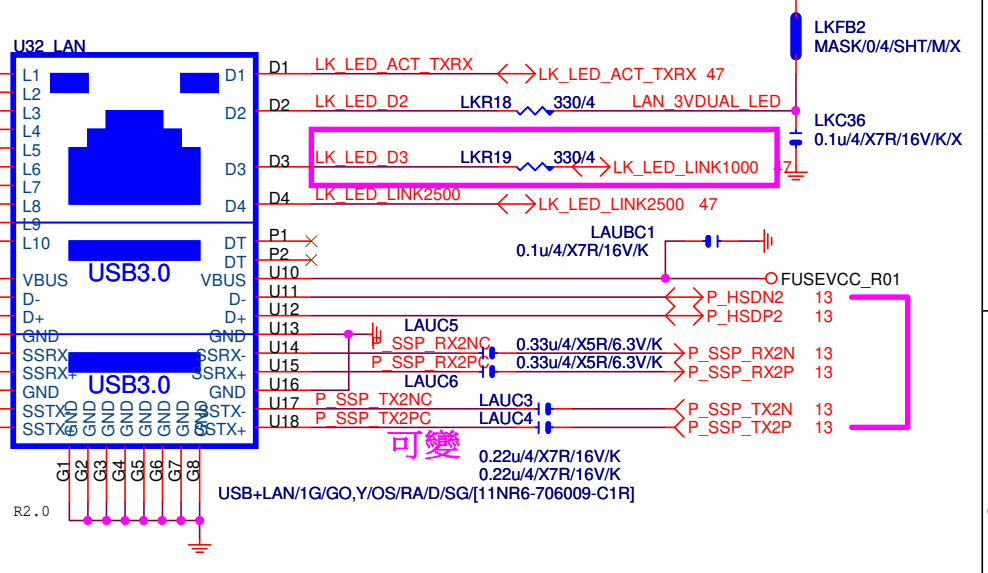


USB_LAN CONNECTOR LA_MDI-->100歐母: [20/4/8/4/20]

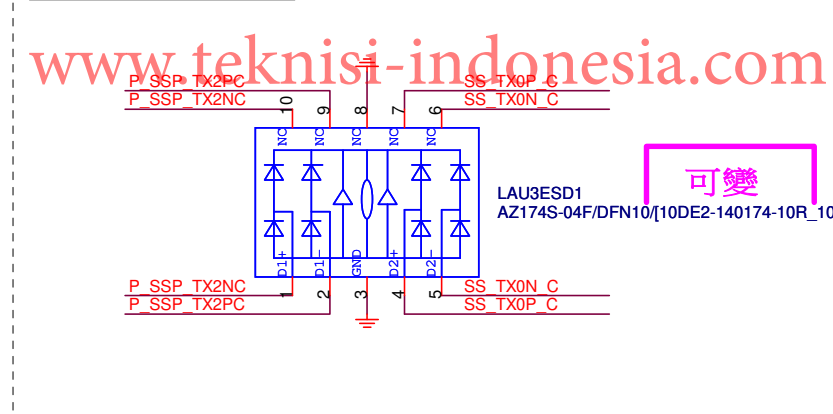


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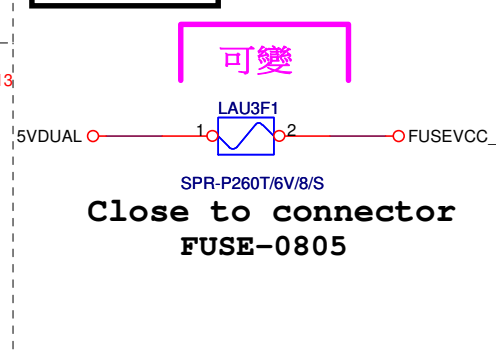
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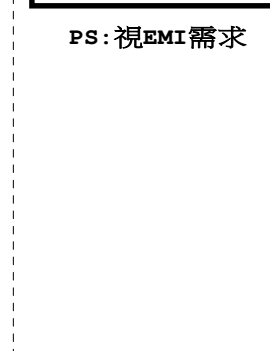
RMA ESD PROTECT note:可變更USB NAME



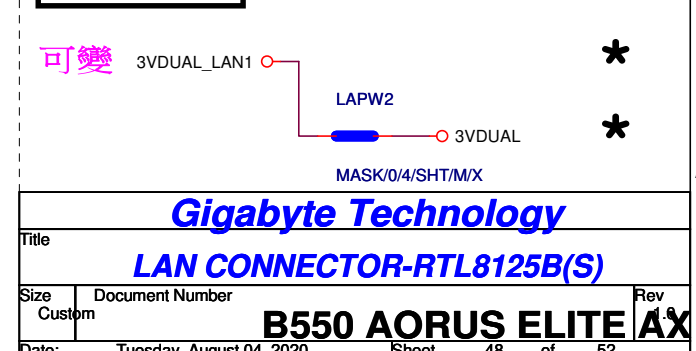
可變



EMI SHORT PAD PS: 視EMI需求

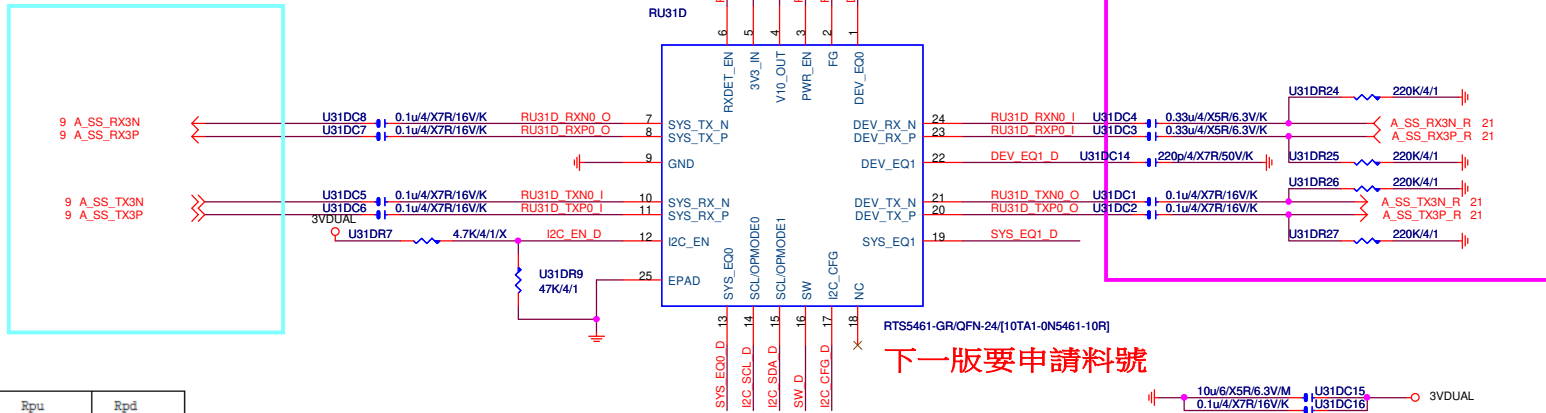


LAN POWER note: lan power連接及電流

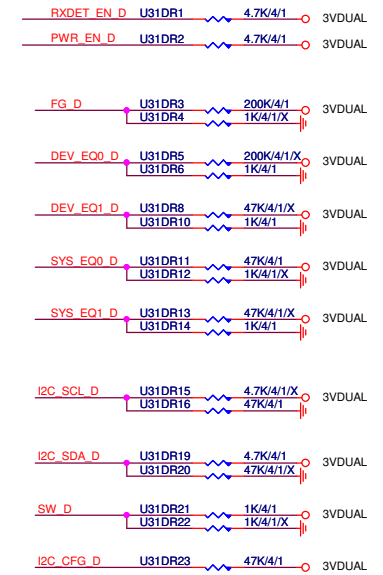


PCH Site

USB TypeA Connector Site



下一版要申請料號



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XXX EQX	Rpu	Rpd
L	NC	1K
ML	200K	NC
MH	47K	NC
H	1K	NC

EQ Setting in Pin Mode		
XXX EQ1	XXX EQ0	EQ(dB)
L	L	
L	ML	
L	MH	
L	H	
ML	L	
ML	ML	
ML	MH	
ML	H	
MH	L	Default
MH	ML	

I2C_CFG	Rpu
3.3V Voltage level logic	47K
1.8V Voltage level logic	1K

SW	Rpu	Rpd
900mVpp	NC	1K
1000mVpp(Default)	200K	NC
1100mVpp	47K	NC
1200mVpp	1K	NC

FG	Rpu	Rpd
-1dB	NC	1K
0dB(Default)	200K	NC
1dB	47K	NC
2dB	1K	NC

I2C Slave Address Setting in I2C Mode		
DEV EQ1	SYS EQ1	7bit Address
L	L	0x10
L	ML	0x11
L	MH	0x12
L	H	0x13
ML	L	0x14
ML	ML	0x15
ML	MH	0x16
ML	H	0x17
MH	L	0x18
MH	ML	0x19
MH	MH	0x1A(Default)
MH	H	0x1B
H	L	0x1C
H	ML	0x1D
H	MH	0x1E
H	H	0x1F

Mode Select	I2C EN	OPMODE0/SCL	OPMODE1/SDA
I2C Mode	H	AS SCL	AS SDA
Pin Mode - USB3.1 (Default)	L	L	H
Pin Mode - disable	L	L/H	L
Pin Mode - debug purpose	L	H	H

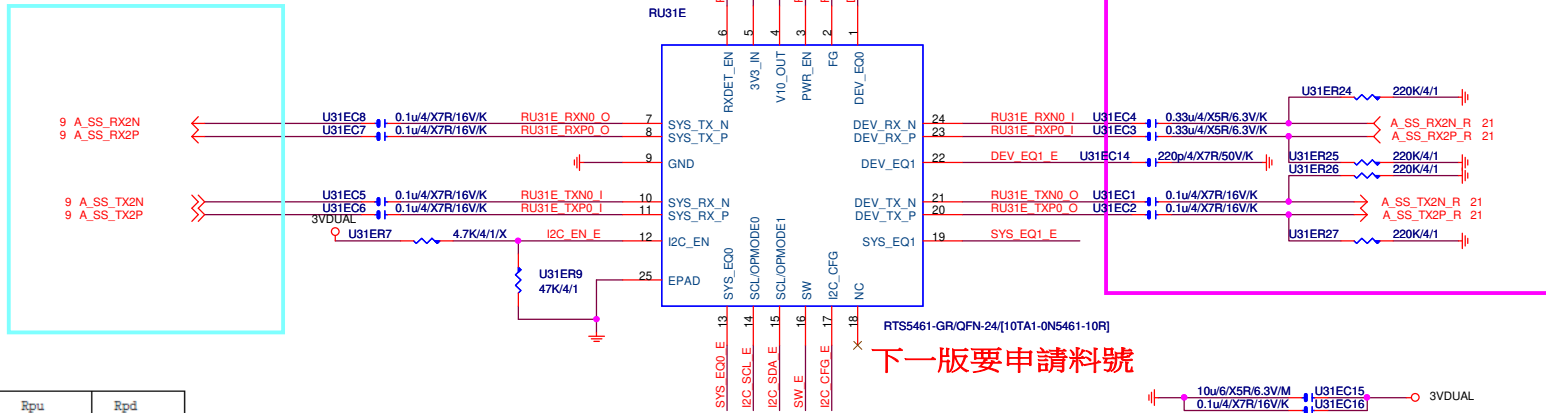
RXDET_EN	
Receiver Detection disable	L
Receiver Detection enable(Default)	H

PWR_EN	
Power Down	L
Power Enable(Default)	H

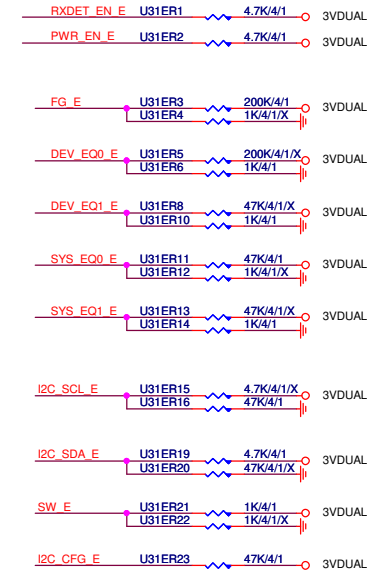
GIGABYTE™			
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PCH Site

USB TypeA Connector Site



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7,16,17,18,36,46,47,49 SMBCLK1
7,16,17,18,36,46,47,49 SMBDATA1

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I2C_CFG	Rpu
3.3V Voltage level logic	47K
1.8V Voltage level logic	1K

SW	Rpu	Rpd
900mVpp	NC	1K
1000mVpp(Default)	200K	NC
1100mVpp	47K	NC
1200mVpp	1K	NC

FG	Rpu	Rpd
-1dB	NC	1K
0dB(Default)	200K	NC
1dB	47K	NC
2dB	1K	NC

Mode Select	I2C EN	OPMODE0/SCL	OPMODE1/SDA
I2C Mode	H	AS SCL	AS SDA
Pin Mode - USB3.1 (Default)	L	L	H
Pin Mode - disable	L	L/H	L
Pin Mode - debug purpose	L	H	H

RXDDET_EN	
Receiver Detection disable	L
Receiver Detection enable(Default)	H

PWR_EN	
Power Down	L
Power Enable(Default)	H

XXX EQX	Rpu	Rpd
L	NC	1K
ML	200K	NC
MH	47K	NC
H	1K	NC

EQ Setting in Pin Mode		
XXX EQ1	XXX EQ0	EQ(dB)
L	L	
L	ML	
L	MH	
L	H	
ML	L	
ML	ML	
ML	MH	
ML	H	
MH	L	Default
MH	ML	

DEV EQ1	SYS EQ1	7bit Address
L	L	0x10
L	ML	0x11
L	MH	0x12
L	H	0x13
ML	L	0x14
ML	ML	0x15
ML	MH	0x16
ML	H	0x17
MH	L	0x18
MH	ML	0x19
MH	MH	0x1A(Default)
MH	H	0x1B
H	L	0x1C
H	ML	0x1D
H	MH	0x1E
H	H	0x1F

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